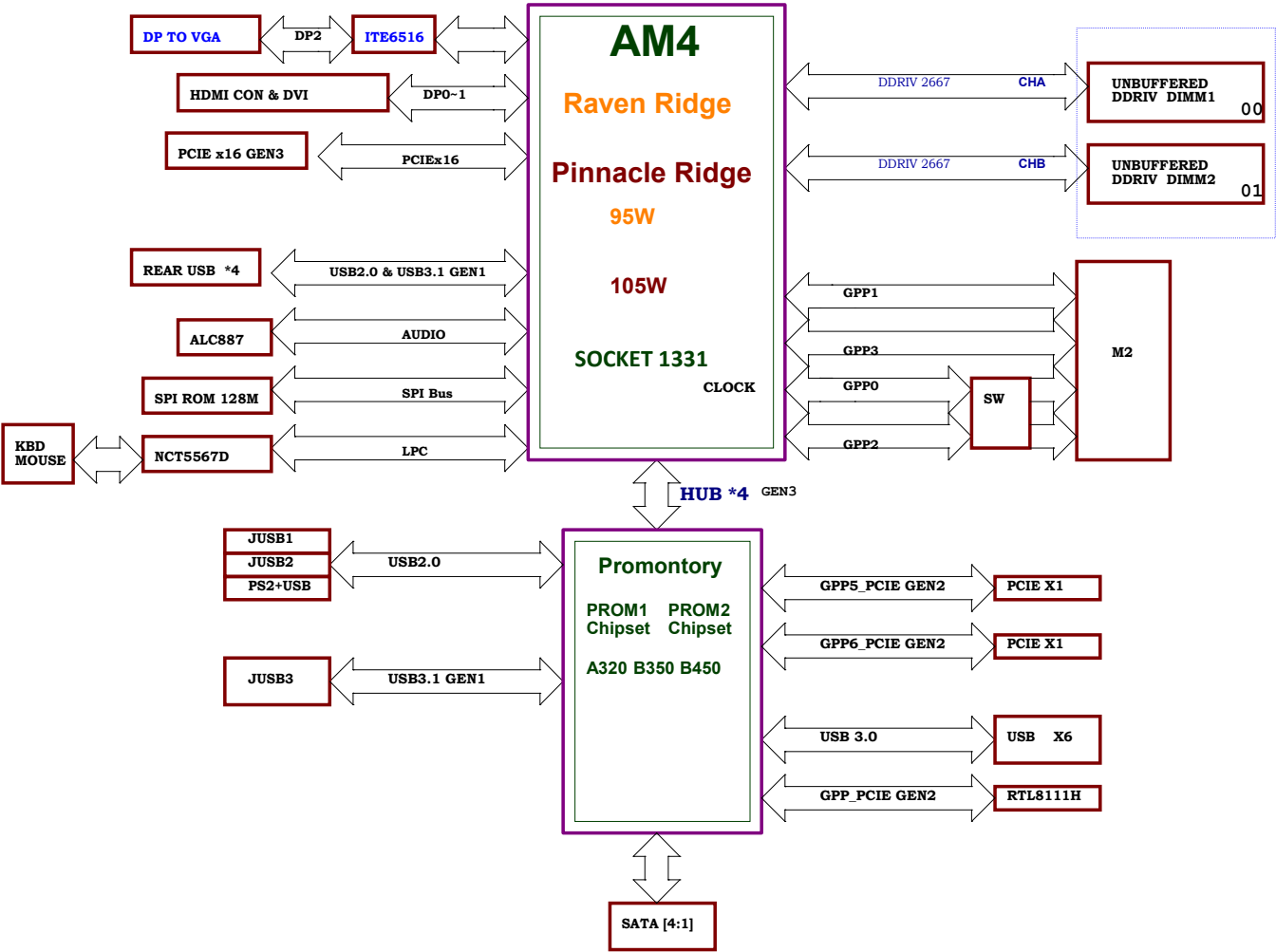


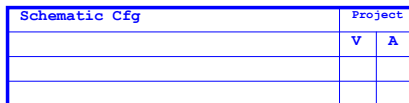
# MS-7B84 Ver:21

- CPU:**  
AMD AM4
- System Chipset:**  
Promontory A320 & B450  
(Value DIY or System Builder)
- Main Memory:**  
DDR IV \* 2 MAX:32 GB
- VRM**  
UP9505 4+2
- On Board Chipset:**  
LPC Super I/O --NCT5567  
LAN RTL8111H  
Azalia CODEC - Realtek ALC887
- Expansion Slots:**  
From CPU  
PCI Express X16 Slot \* 1  
PCI Express X1 Slot \* 1  
PCI Express X1 Slot \* 1  
M2\_2 \* 1
- OCF IC:**  
RT9553B

## FUSION BLOCK DIAGRAM



01 Block Diagram	37 CPU Power VDDP-MP8712
02 Cover Sheet	38 CPU Power Connector/PWRGD
03 FM4 DDR4 I/F	39 CPU Power RT8894 3+2 Phase
04 AM4 PCIE/SATAE	40/41 CPU Power Phase 1-4
05 AM4 Display/Audio	42 CPU Power NB Phase 1-2
06 AM4 SVI/ACPI/GPIO	43 CPU Power NB Switch/NCT3933
07 AM4 LPC/SPI/USB/CLK/STRAP	44 RT9553B CURRENT SENSE
08 AM4 Power/RTC Power/ 09 AM4 GND	45 ATX/Front Panel
10,11 DDR4-DIMM CH-A/B	46 ALL LED Control
12,13 DDR4-POWER/GND	47 BOM Option
14 Promontory-PCIE/SATA/SATAE	48 RTC Circuit/Moat Cap
15 Promontory-USB/OC	49 M2_2
16 Promontory-CLK/ACPI/GPIO	50 History
17 Promontory-Power / 18 Promontory-GND	51 Power Sequence
19 PCIE X16(X1*2) SLOT	52 Power Delivery
20 SIO NCT5567D	53 GPIO MAP
21 DVI Connector	
22 CPU/SYS FAN Control TYPE K	
23 / 24 / 25 LAN-RTL8111H/Audio ALC887	
26 USB Rear PS2+USB2.0	
27 USB Rear LAN+USB3.1 GEN1	
28 USB Front Side	
29 SATA Connector	
30 HDMI Connector	
31 DP to VGA RTD2166	
32 ACPI uPI-5VDIMM&3VSB	
33 PM-SY8288RAC-1.05V/GS7133-2.5V	
34 DDR PWR VPP25/VTM-MP2147	
35 DDR Power-RT8231AGQW	
36 CPU Power 1P8V-MP2147	



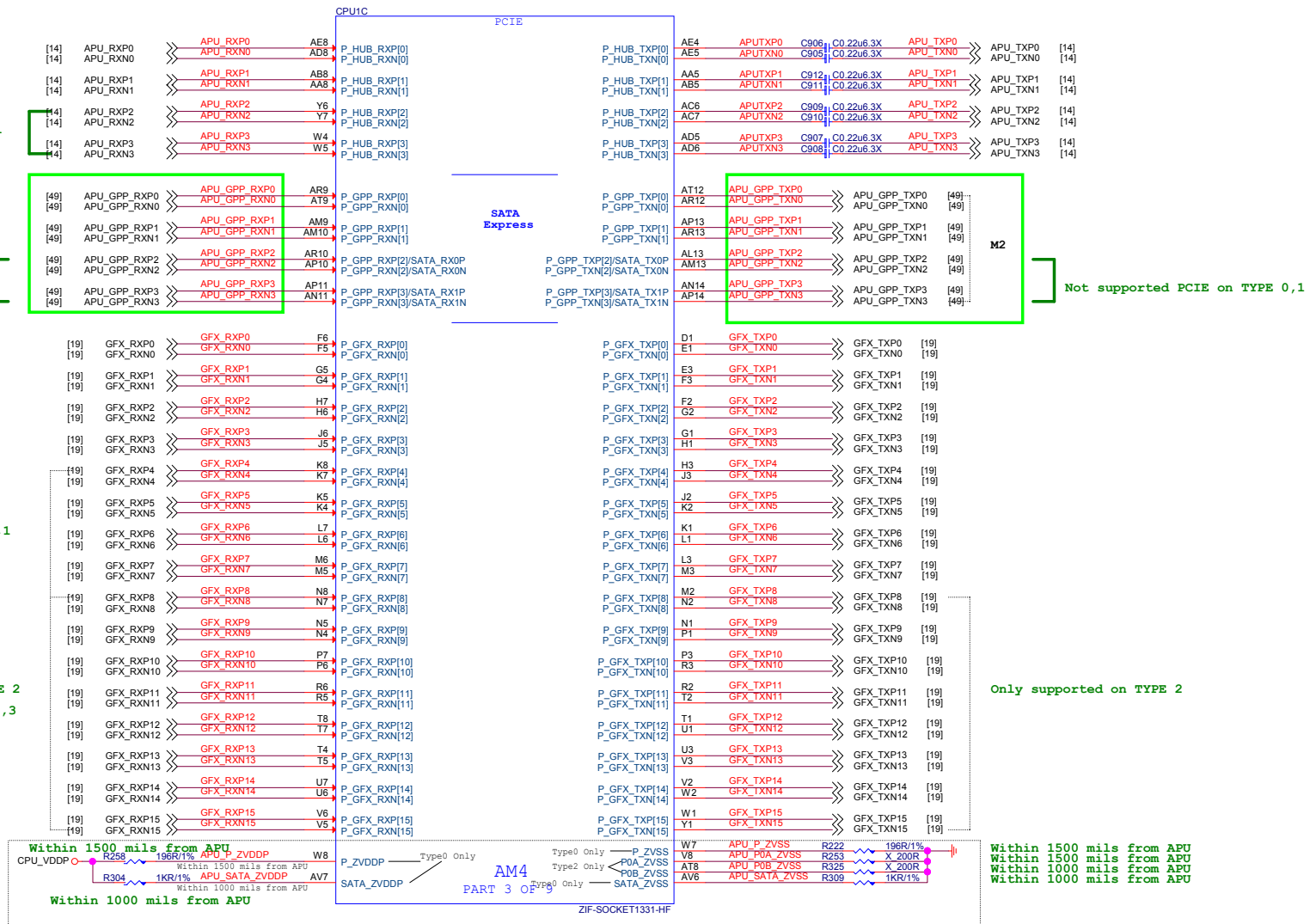
Not supported HUB on TYPE 1

Not supported PCIE on TYPE 0,1

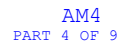
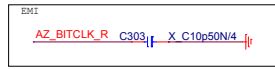
TYPE 0	PCIE	SATA
TYPE 2/3	2 or 4	2 or 0

Not supported GFX 4~15 on TYPE,1

Only supported on TYPE 2  
Not supported GFX 8~15 on TYPE 0,3



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For DVI

→ Not supported on TYPE 2

```
AM4 Type 1 processors: DP2 is not supported
50724 1 13
```

For DP to VGA RV2 AM4 35W is a de-featured version of RV1 AM4 65W, RV2 AM4 35W can only support 2 displays

Here is the example of Raven2 AM4's DP2 function on existing AM4 board :

- 1.D-sub : DP to VGA translator (e.g. ANX62xx) ok
- 2.DP : only 2 lanes can work (lane 0 and lane1)
- 3.DVI-D : no display (no TMDS clock on lane3)
- 4.HDMI : no display (no TMDS clock on lane3)

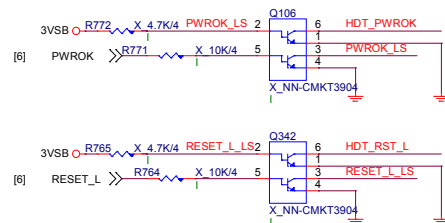
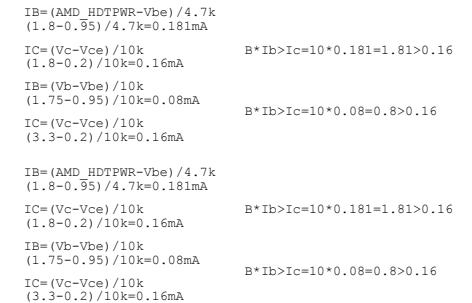
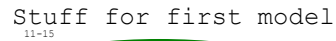
by mail 2017-11-28

Type0 Only

For Debug2

Not support Type2

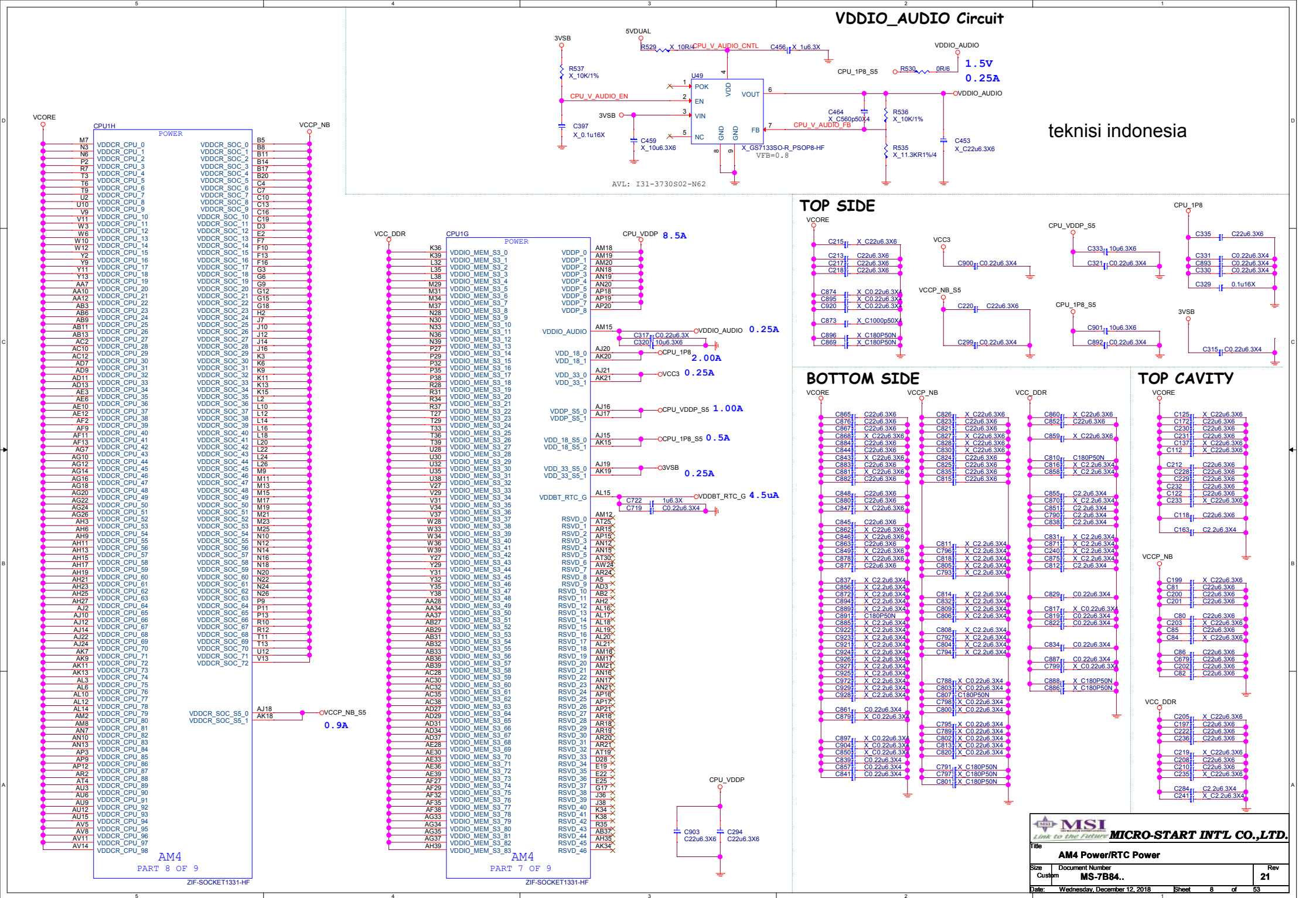
K14 PIN: 不管SPEC有沒有HDMI,都需PU HIGH,  
這樣使用DVI轉HDMI Dongle,接上HDMI螢幕才會有聲音輸出



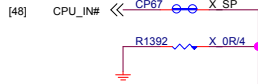













GND

AM4  
PART 9 OF 9

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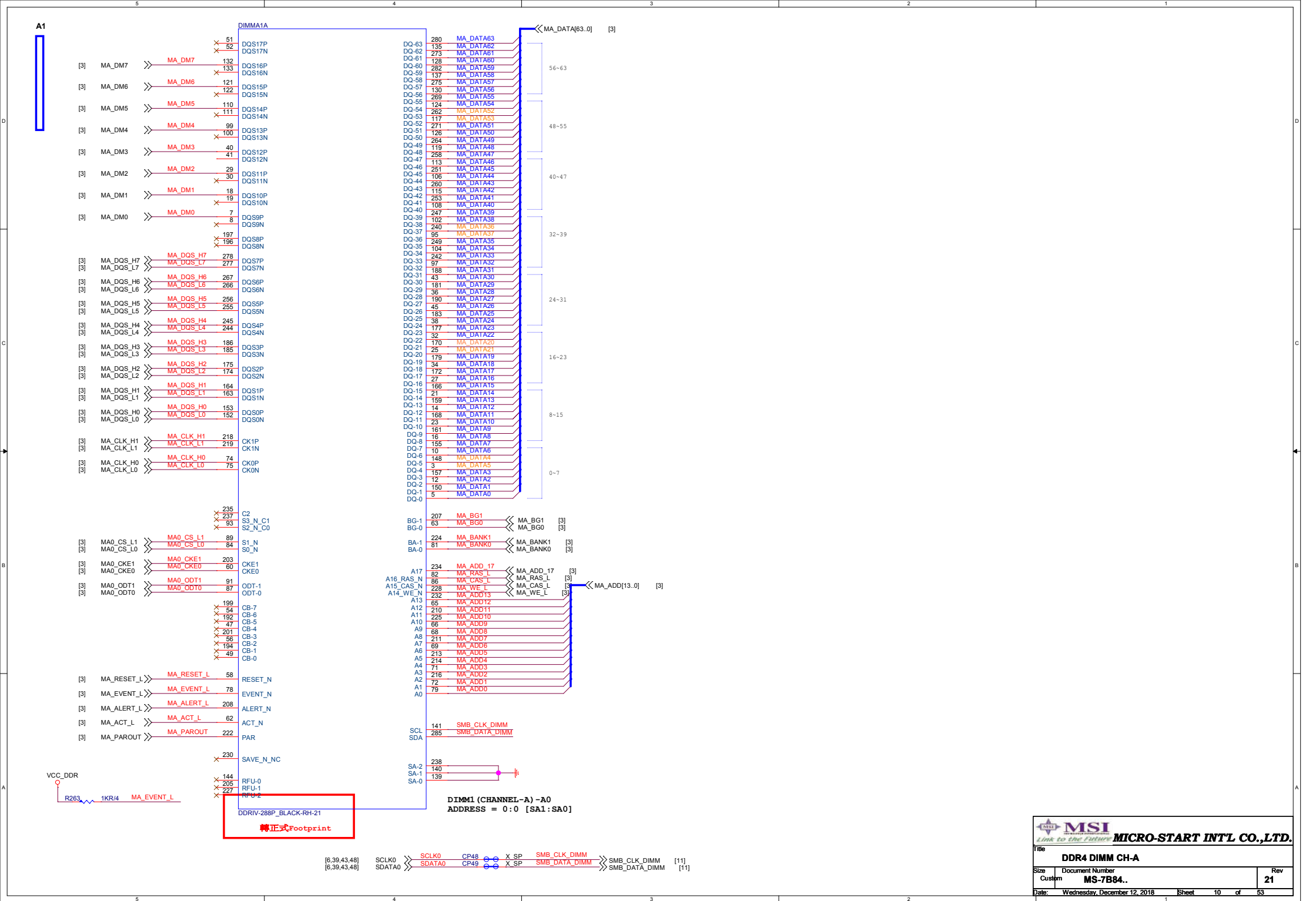


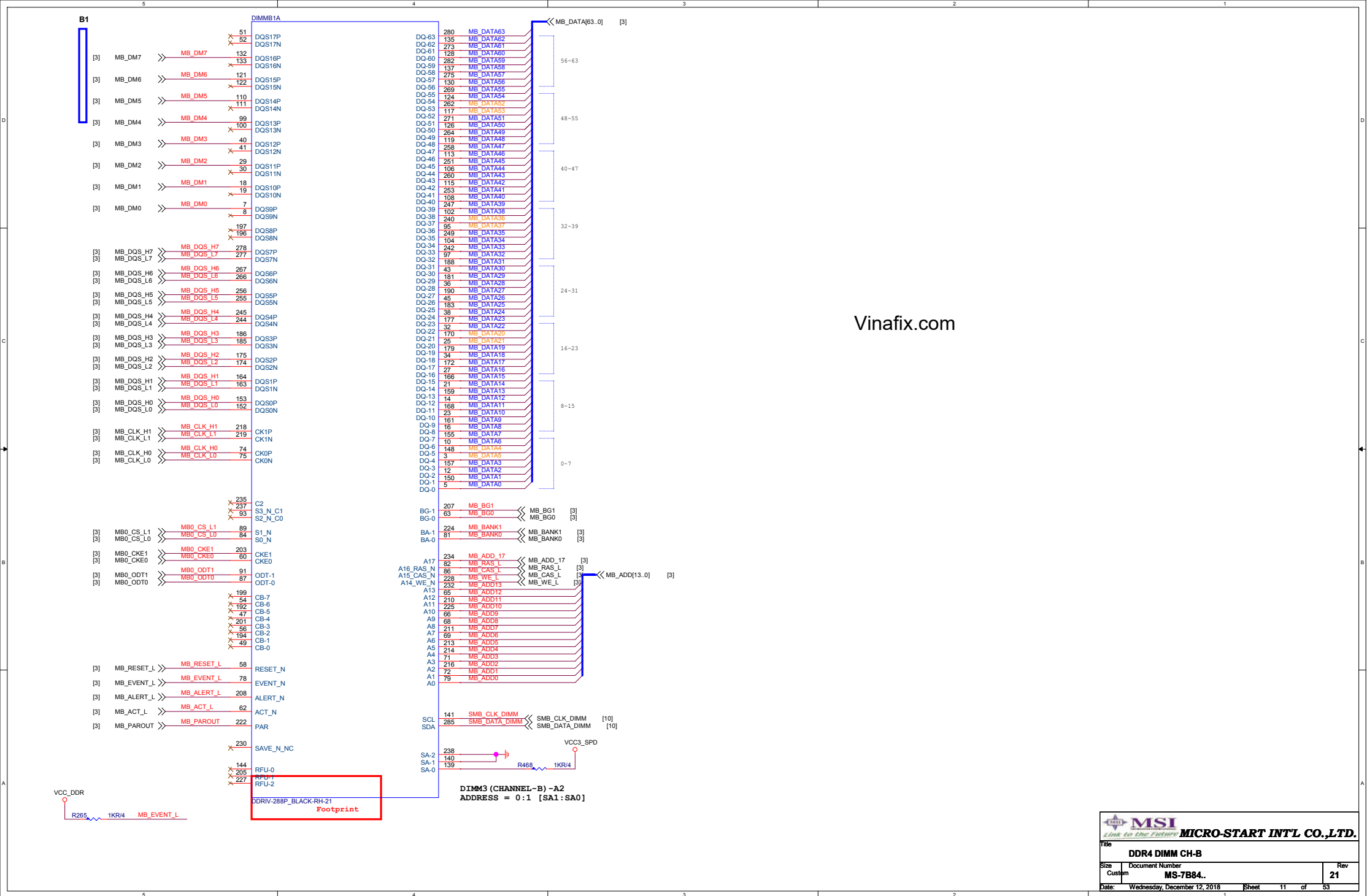
**MICRO-START INT'L CO.,LTD.**

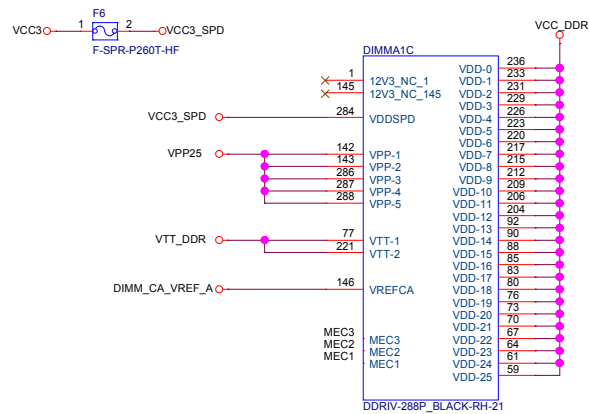
Title: **AM4 GND**

Size: Custom	Document Number: <b>MS-7B84..</b>	Rev: <b>21</b>
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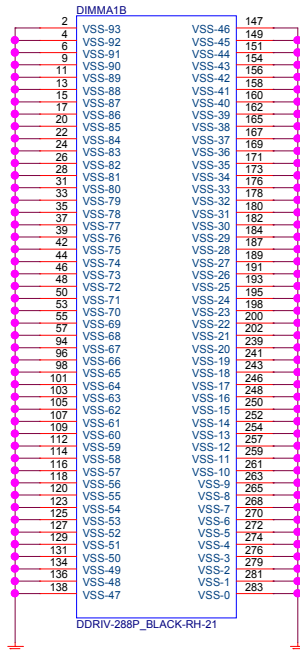
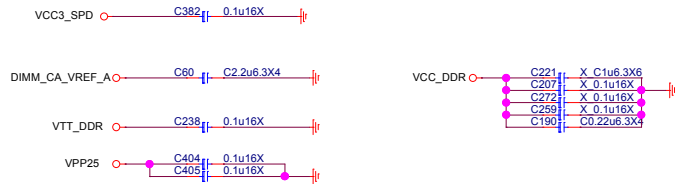
Date: Wednesday, December 12, 2018 Sheet 9 of 53





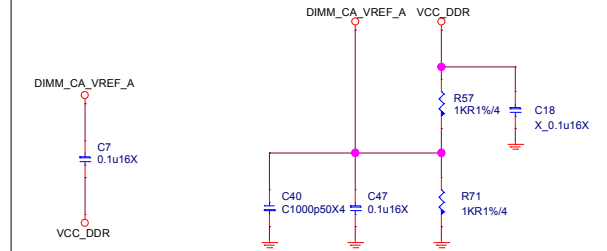


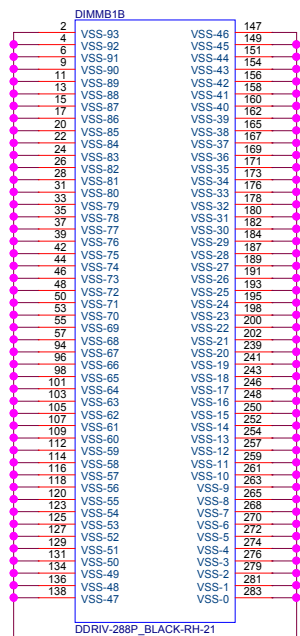
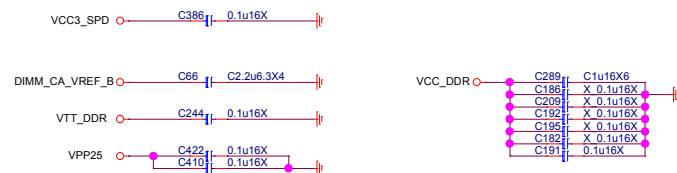
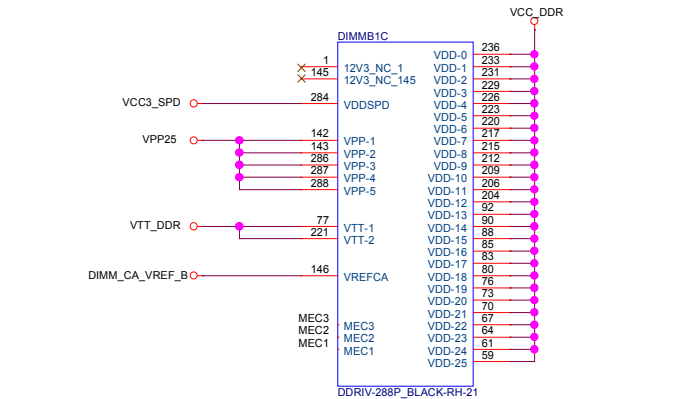
DIMM SLOT PN BY SPEC



## DDR VREF

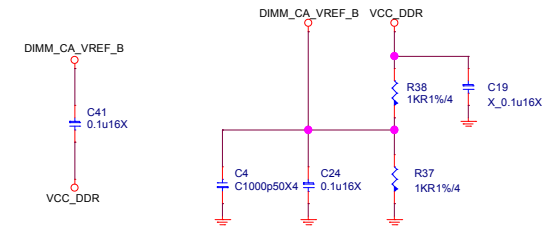
(place resistors close to DIMMs)



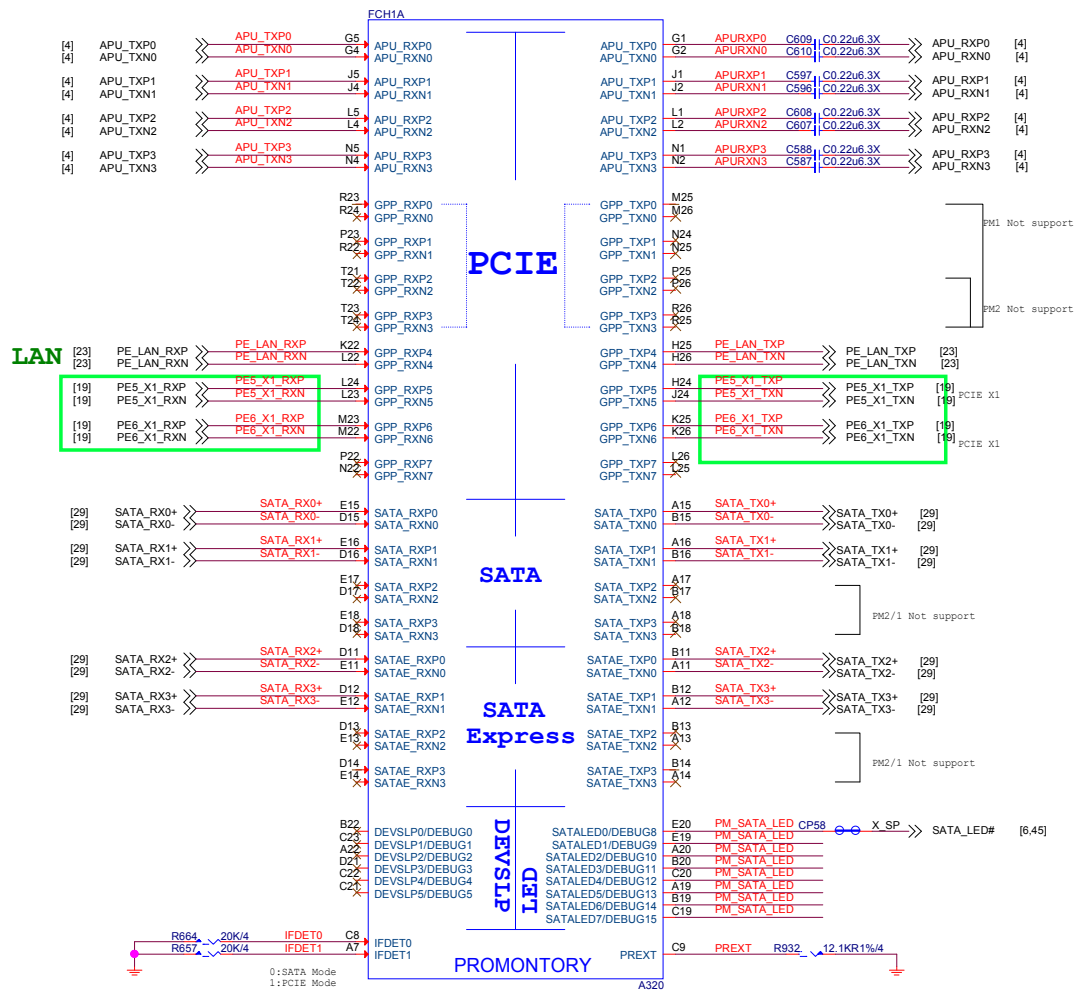


## DDR VREF

(place resistors close to DIMMs)

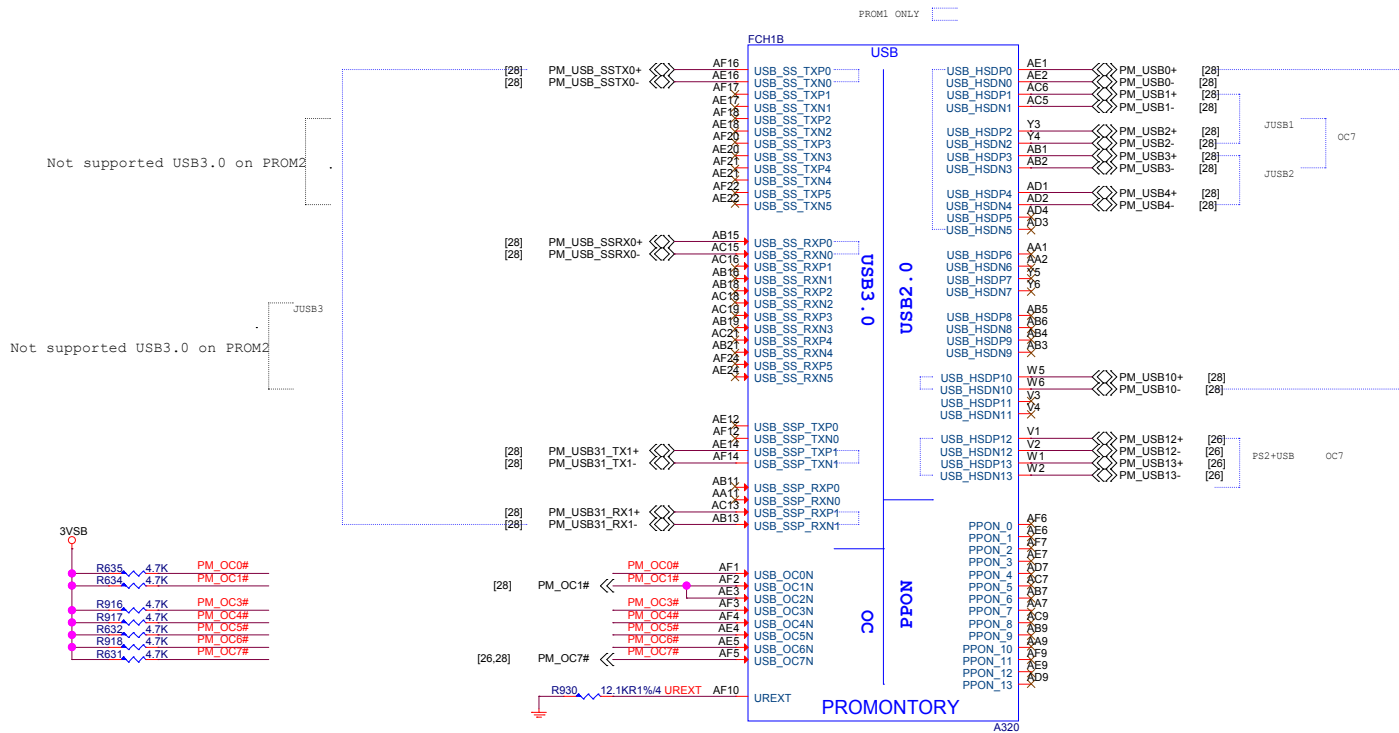






SATA Express port0 (IFDET0)  
SATA Express port1 (IFDET1)  
0:SATA Mode  
1:PCIe Mode

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## Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

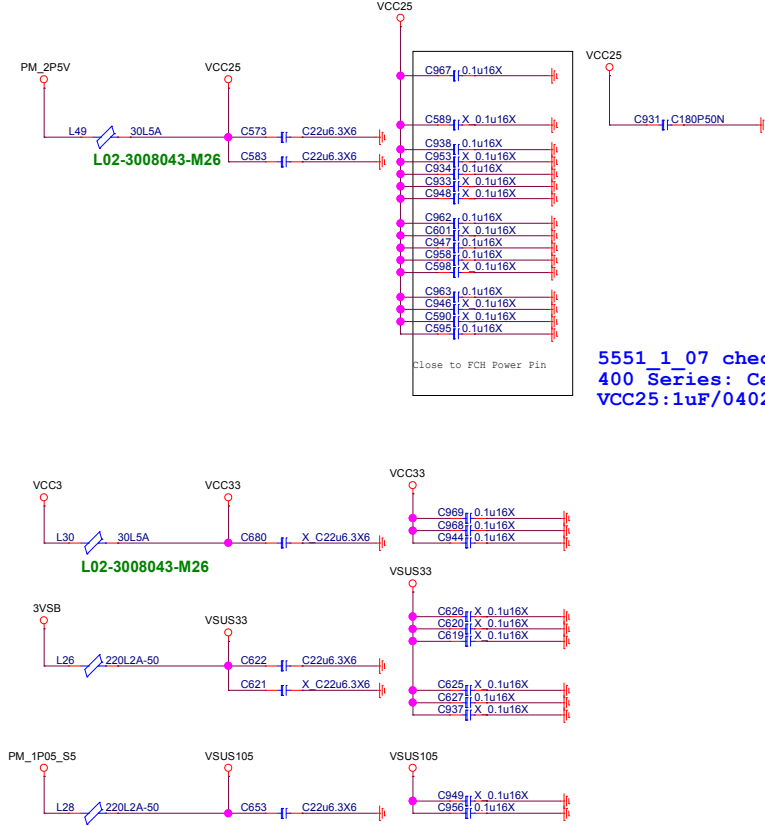
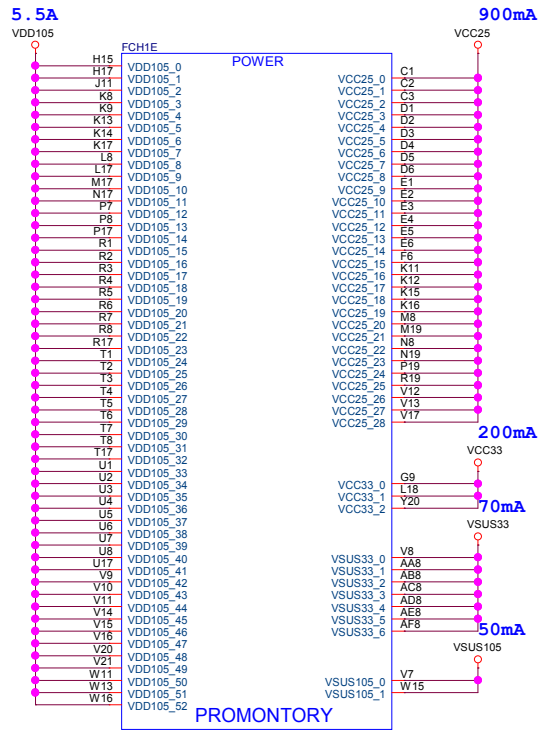
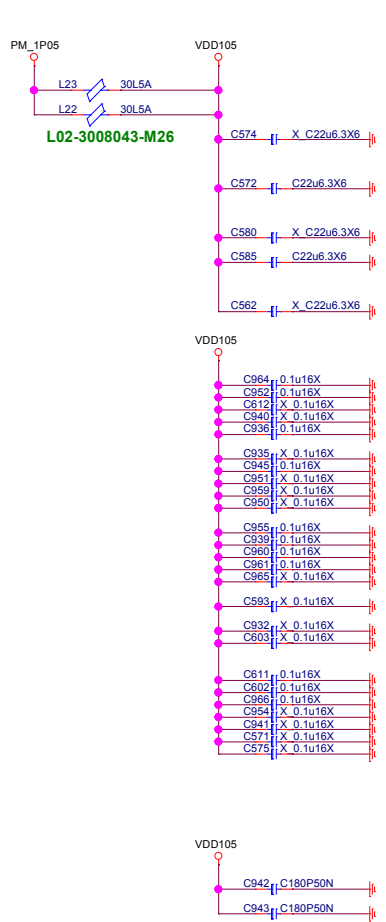
## Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~3	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

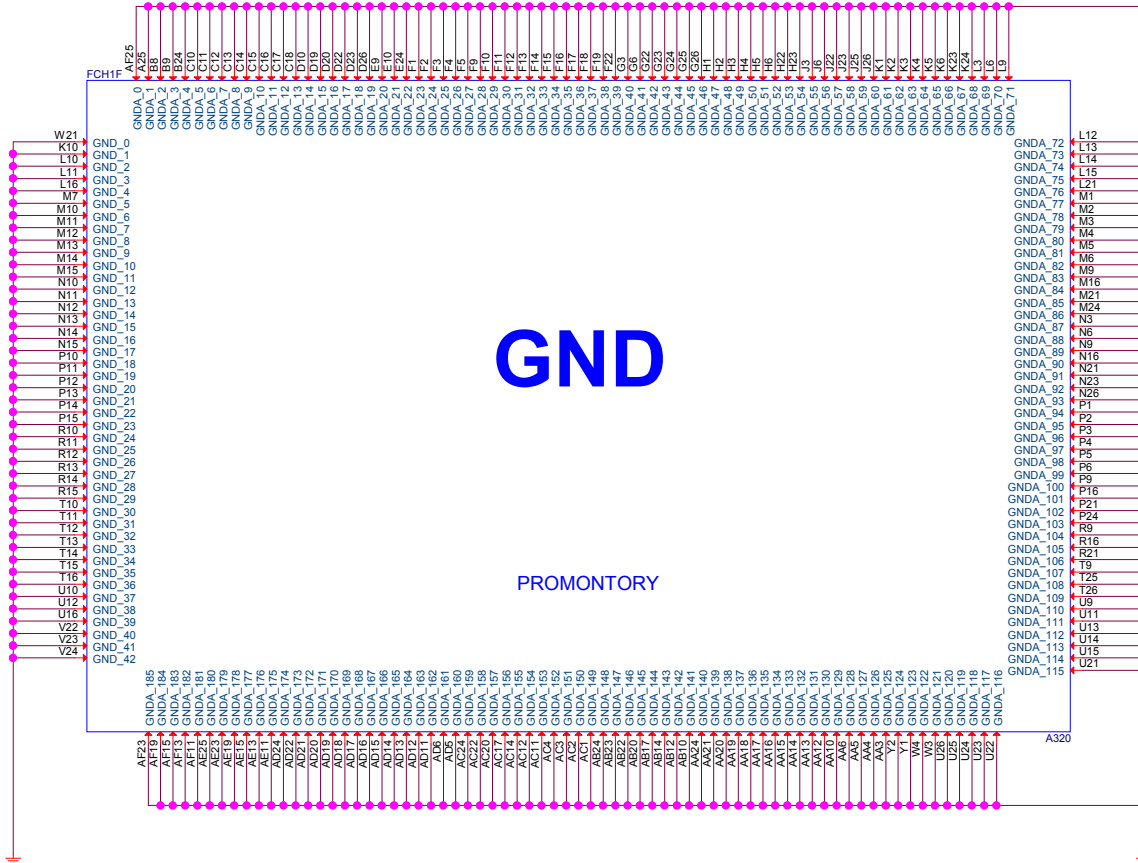
CLK2.3不能用  
CLK1-3不能用





5551\_1\_07 check list  
400 Series: Ceramic capacitors.  
VCC25:1uF/0402





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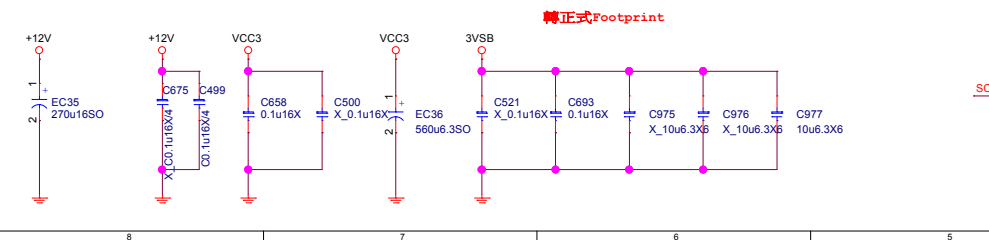
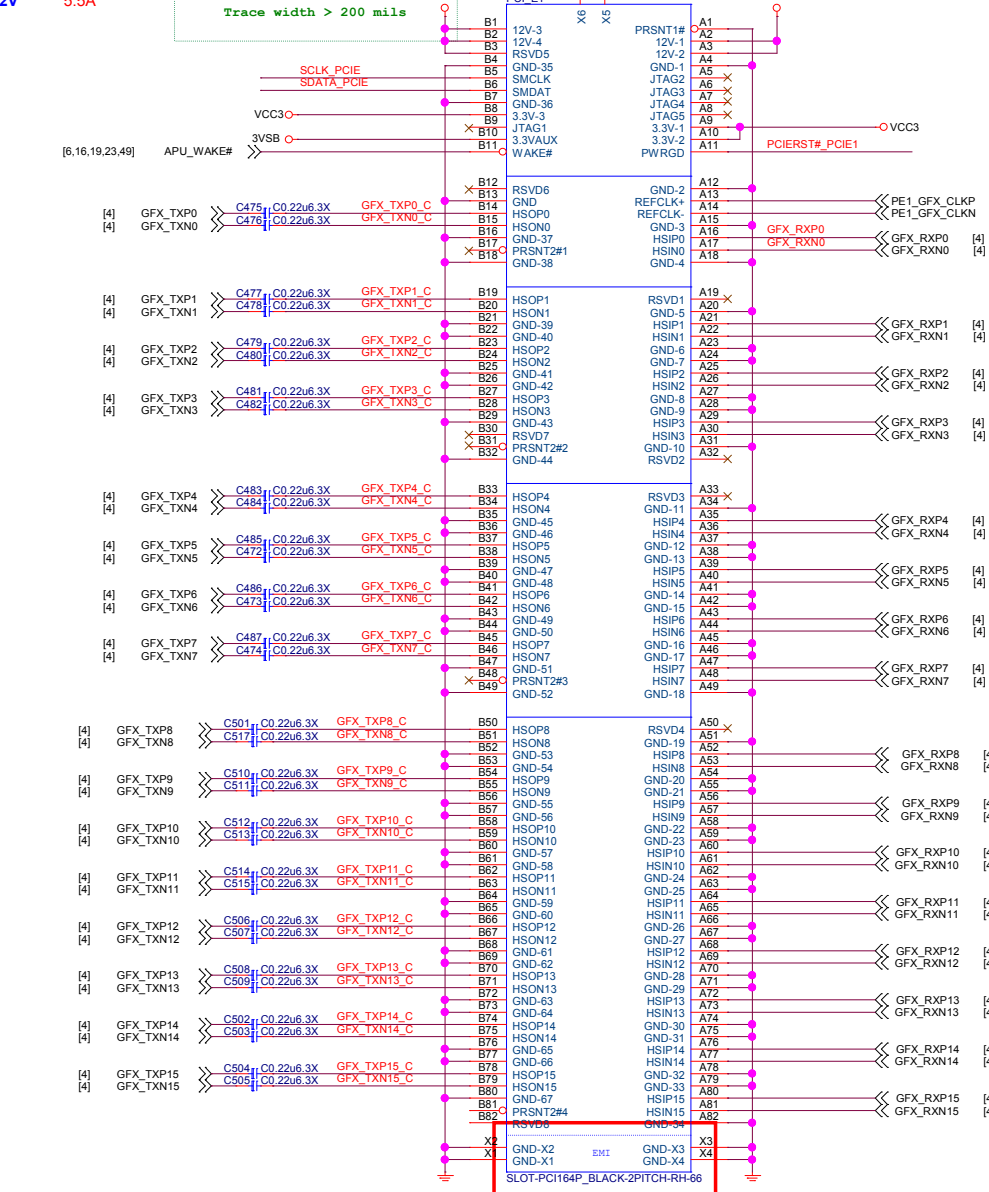


PCI EXPRESS x16 Slot

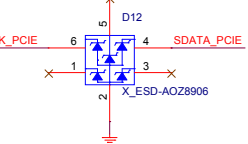
3.3V 12V 3.0A 5.5A

PCIEX1 12V 0.5A 3.3V weak 375mA

3.3V 12V 3.0A 0.5A



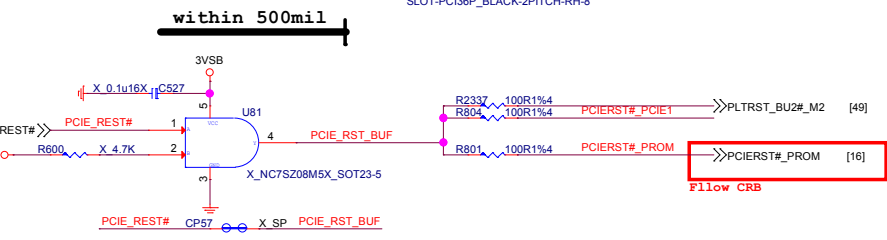
正式Footprint



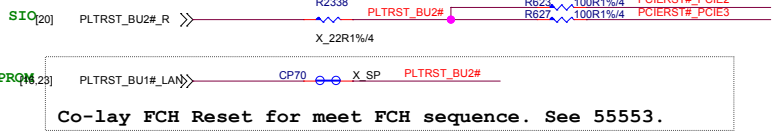
SMBus separate circuit

SMB\_SEL GPIO Default High

SCLK\_PCIE SDATA\_PCIE



PROM RESET



Co-lay FCH Reset for meet FCH sequence. See 55553.

within 500mil

MSI MICRO-START INT'L CO.,LTD.

Title: PCIE X16(X1\*2) SLOT

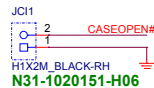
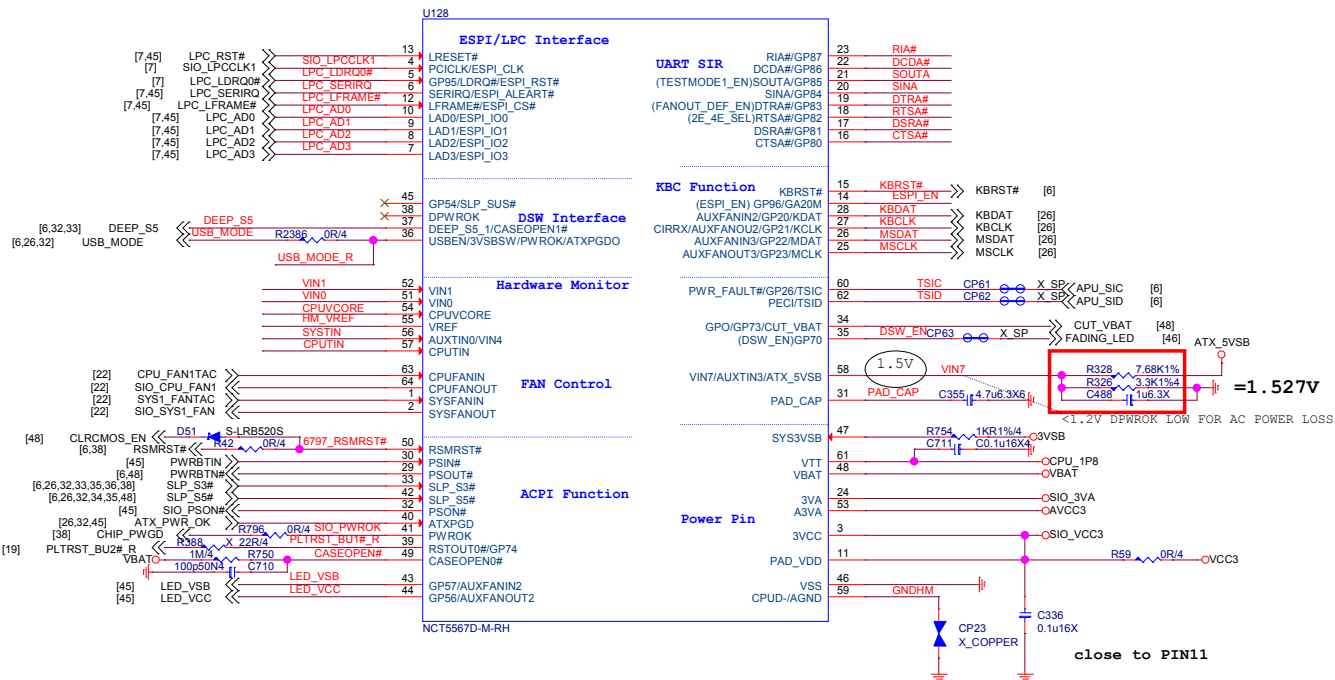
Size: Custom

Document Number: MS-7B84..

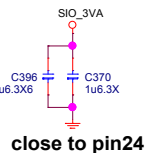
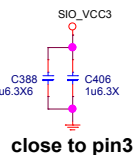
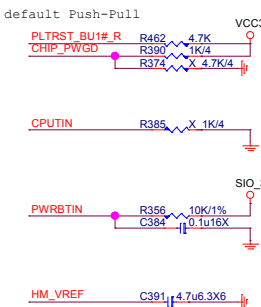
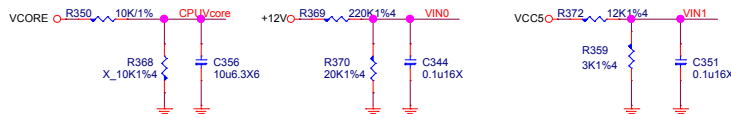
Date: Wednesday, December 12, 2018

Sheet: 19 of 53

Rev: 21

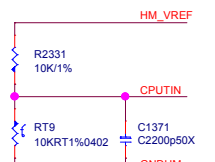


## HW Monitor - Voltage

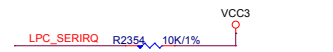
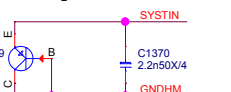


## Thermal Monitor

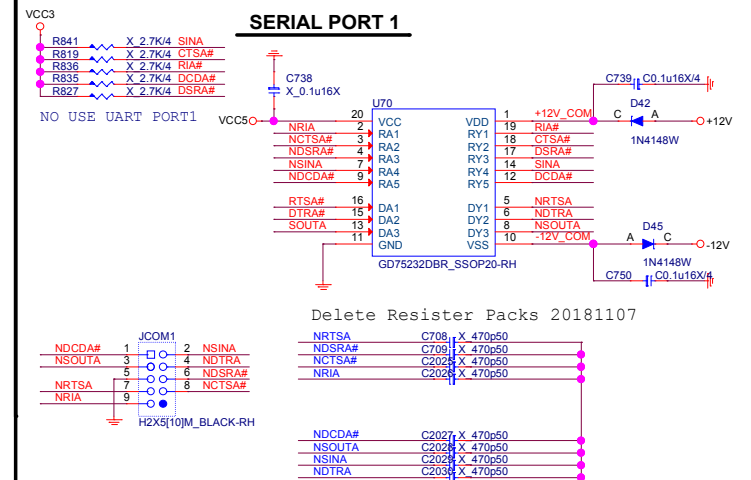
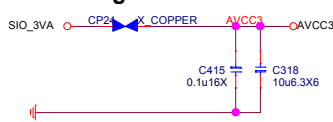
For CPU Under Socket



For System Close to SIO



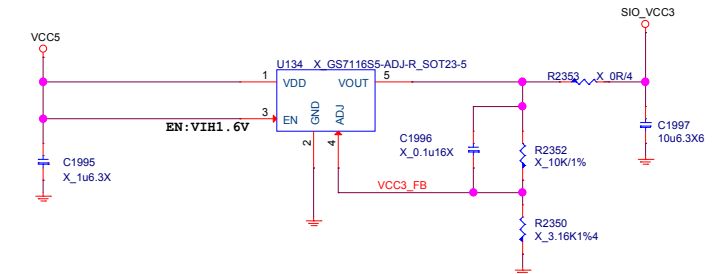
## 3V Analog Power



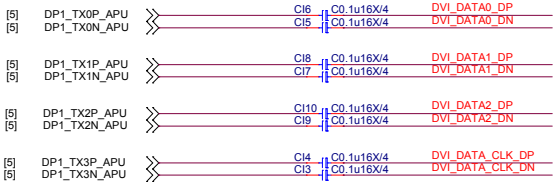
## POWER ON STRAPPING PIN FOR NCT5567D

PIN	5567D NAME	Circuit NAME	0	1
18	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E
19	FANOUT_DEF_EN	DTRA#	default 50%	default 100%
21	TESTMODE1_EN	SOUTA	DISABLE TEST1MODE	ENABLE TEST1MODE
14	ESPI_EN	ESPI_EN	ENABLE LPC	ENABLE ESPI
35	DSW_EN	DSW_EN	GPIO function	DSW function

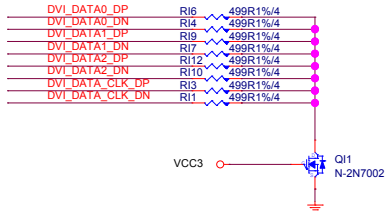
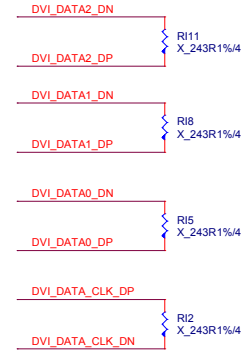
## teknisi indonesia



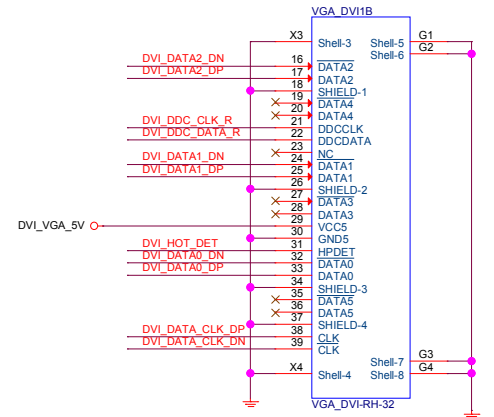
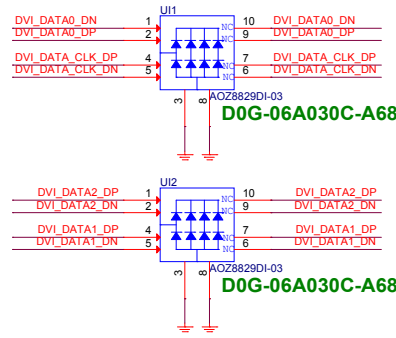
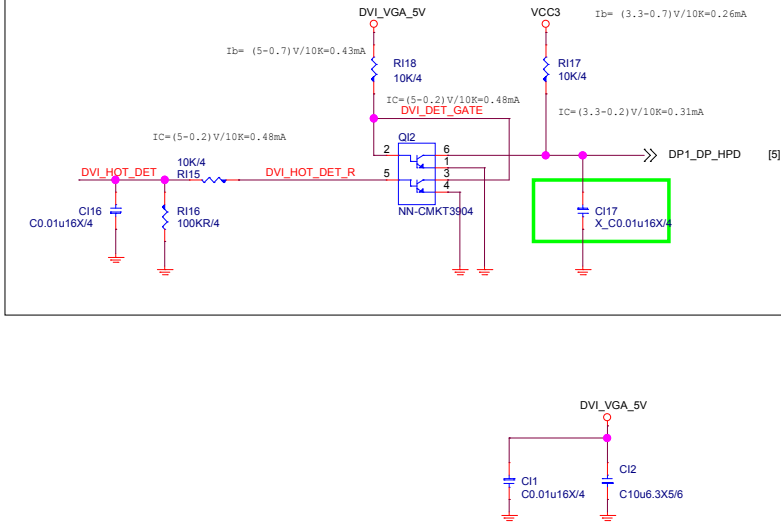
# DVI CONNECTOR



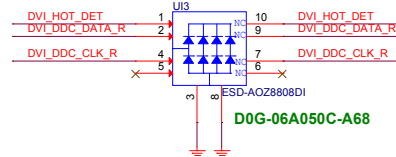
## For EMI



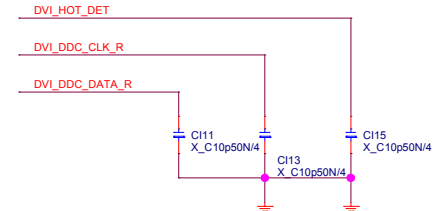
## HPD



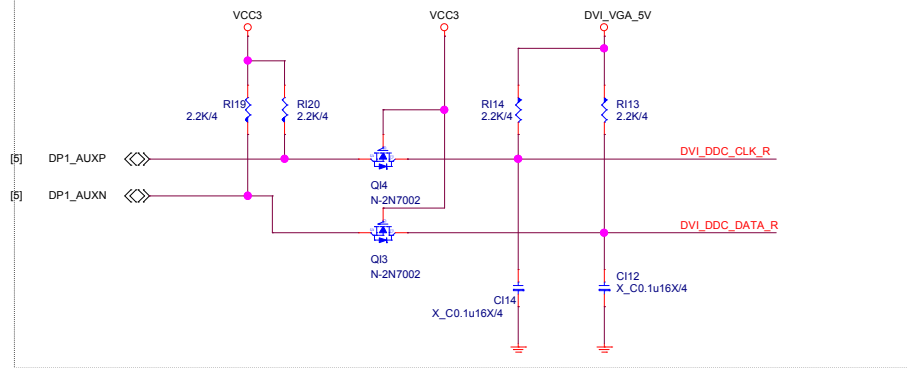
## 注意:耐壓5v零件



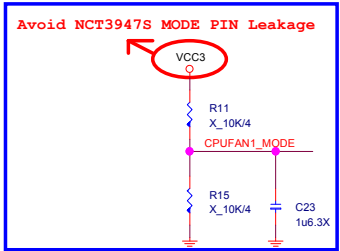
## For EMI



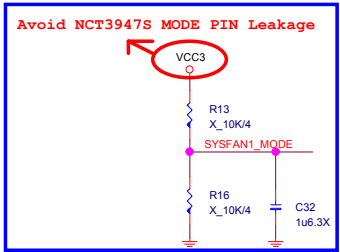
## LEVEL SHIFT using I2C Repeater



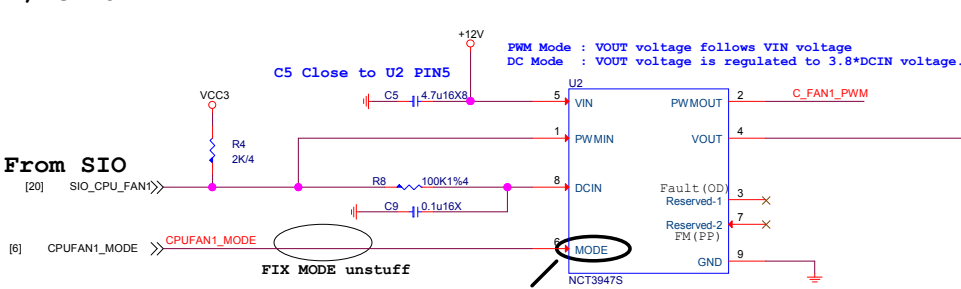
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE  
2.GPIO 由BIOS PWM/DC MODE



Resever For FIX DC or PWM MODE USE By FM SPEC



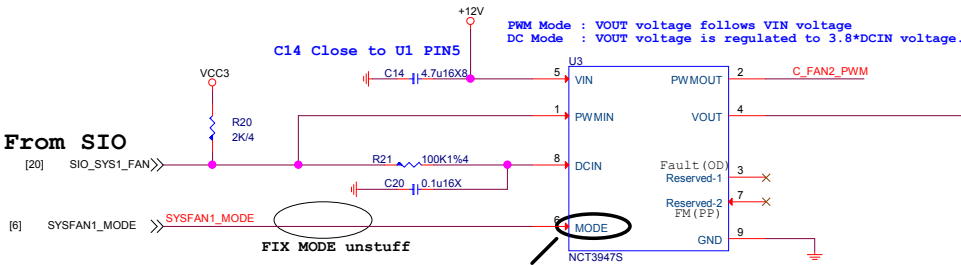
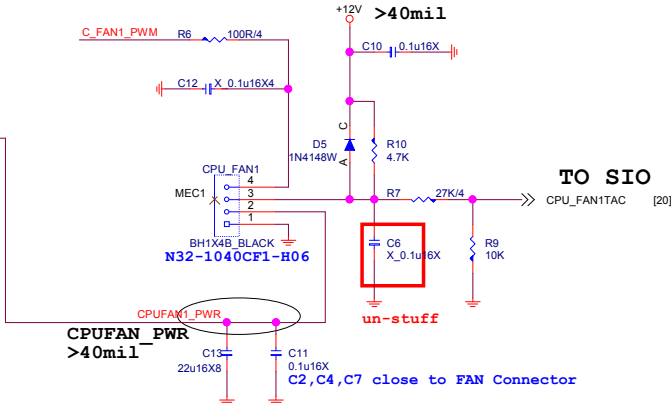
Resever For FIX DC or PWM MODE USE By FM SPEC



GPIO Control

	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

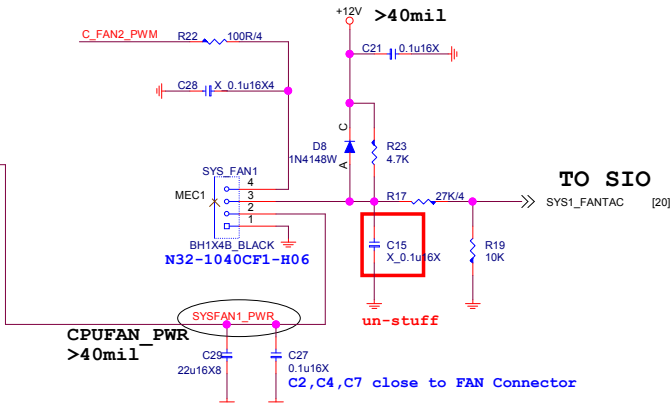
Default Internall pull up 1.65V



GPIO Control

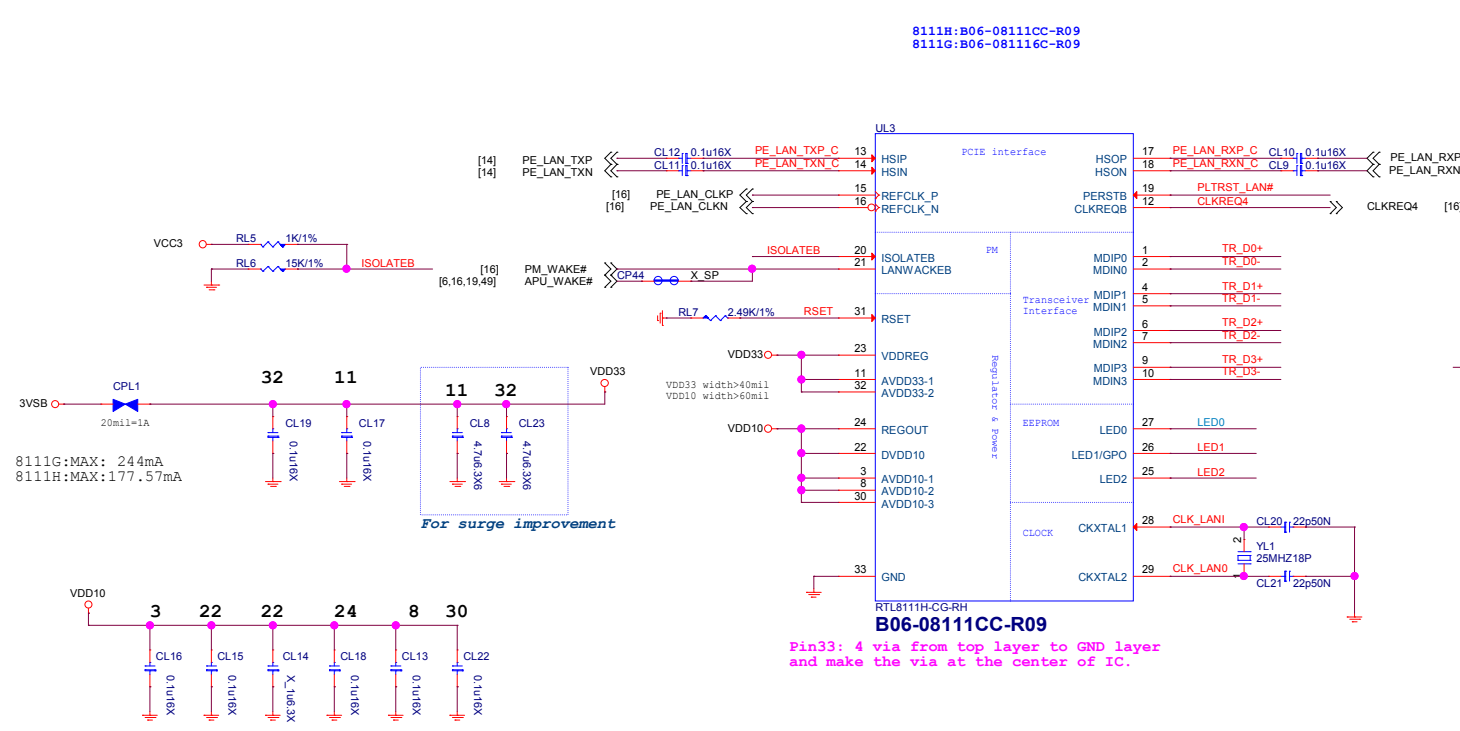
	MODE (PIN7)
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating)

Default Internall pull up 1.65V



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RTL8111G/RTL8111H Giga LAN

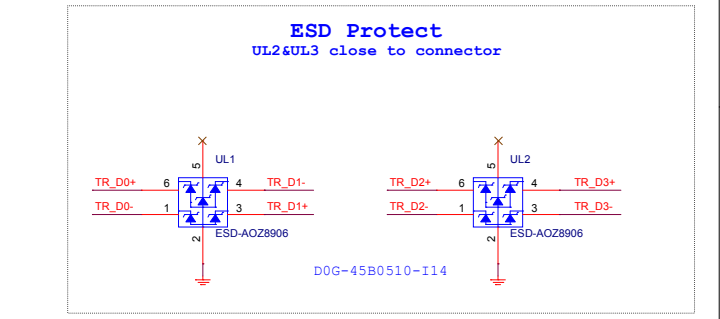
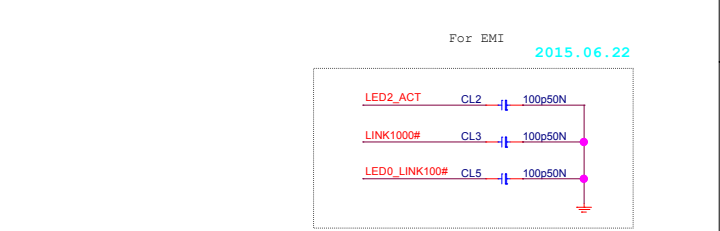
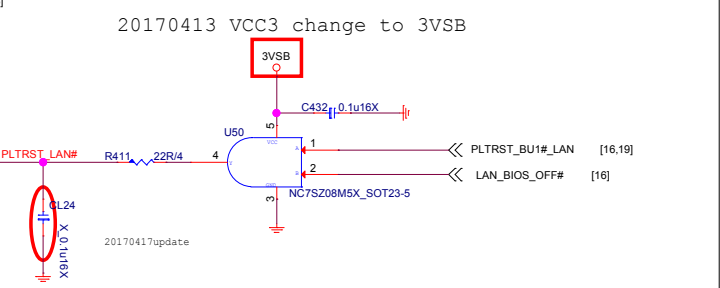
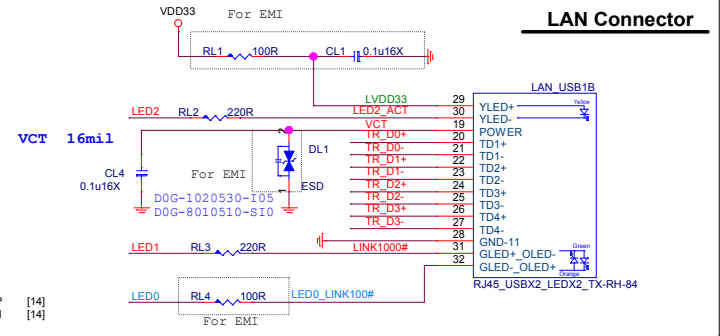


8111G POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	17.15/116.7	56.6/385.1
100 M Idle/TxRx	71.45/129.5	235.8/427.4
Giga Idle/TxRx	179.1/243.9	591/804.9
ALDPS	6.41	21.15

8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15



MSI MICRO-START INT'L CO.,LTD.

Title: LAN-RTL8111H

Size: Custom

Document Number: MS-7B84..

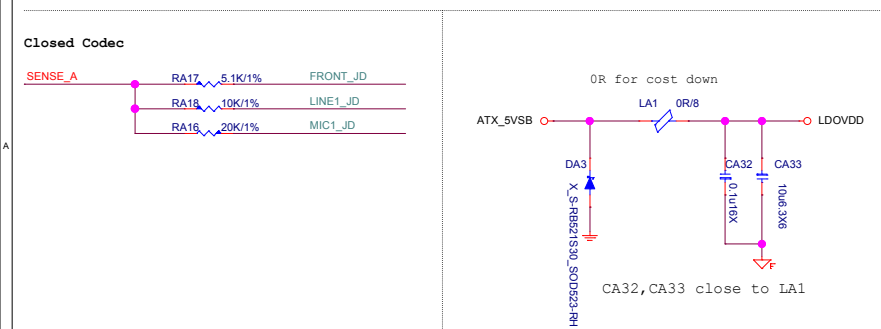
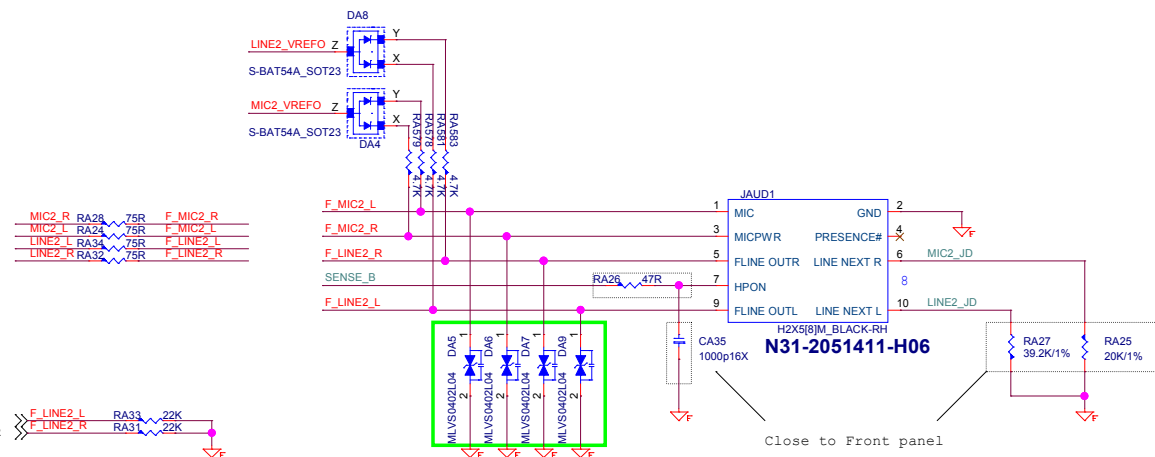
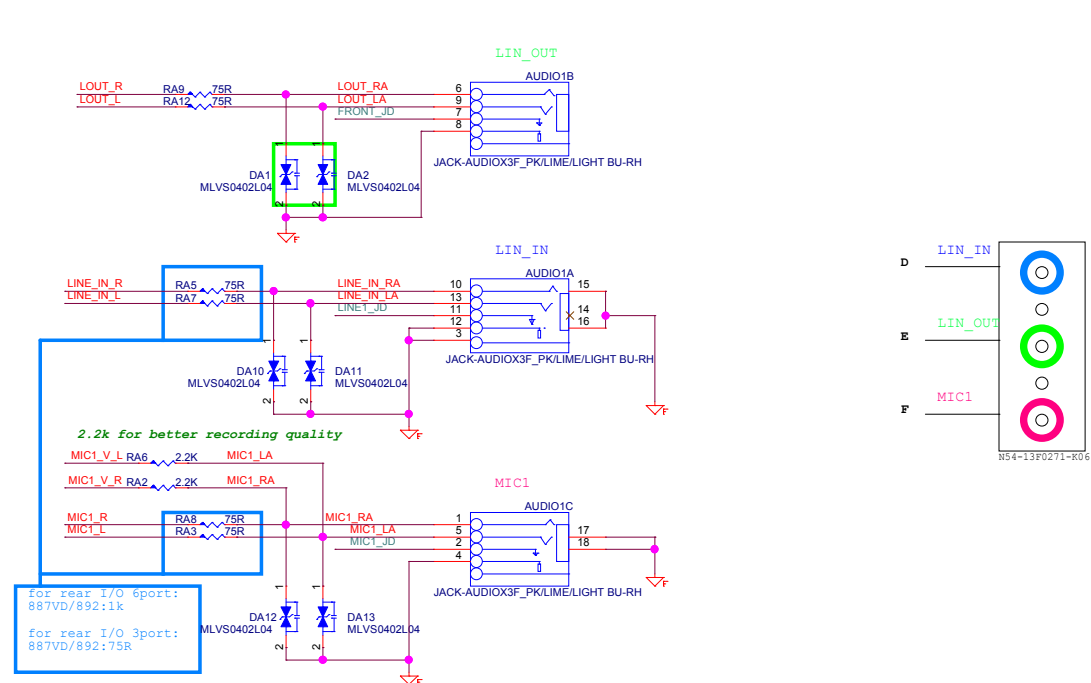
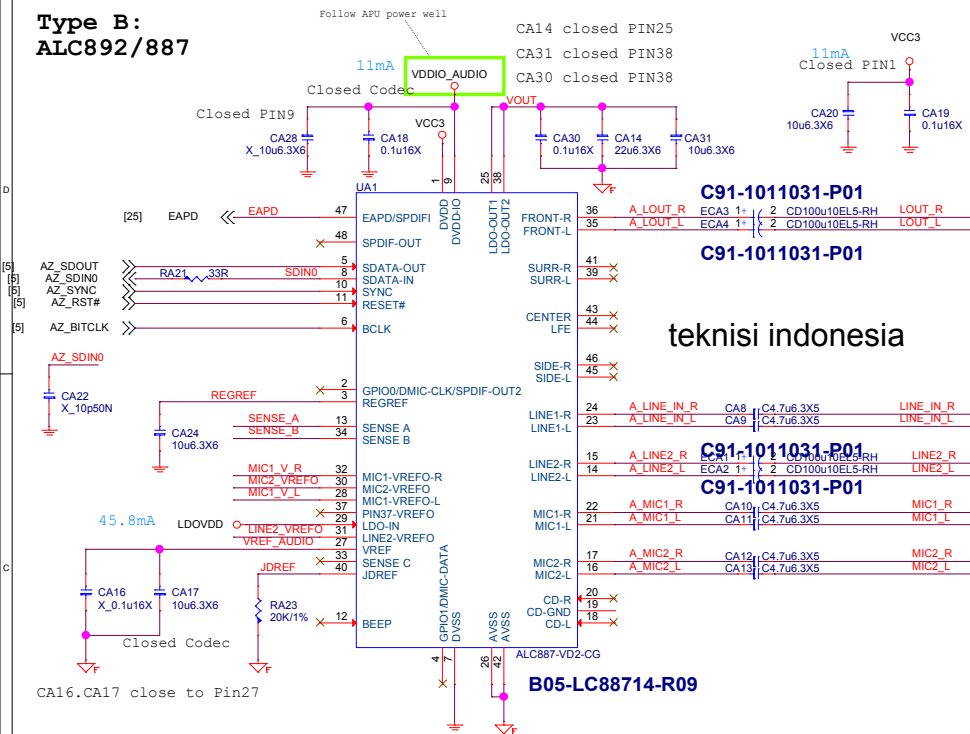
Date: Wednesday, December 12, 2018

Sheet: 23 of 53

Rev: 21



Type B:  
ALC892/887



Varister --> cap for cost down

D0G-2710510-I05

D0G-2950500-SI0

Close to Jack

Close to Front panel  
For HDA/AC97 front cable.

 **MSI**  
Link to the Future **MICRO-START INT'L CO.,LTD.**

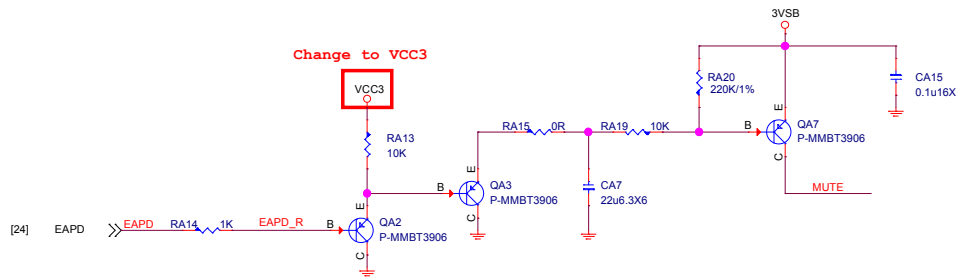
Title	Audio ALC887-1
-------	----------------

Size	Document Number	Rev
Custom	<b>MS-7B84..</b>	<b>21</b>

Date: Wednesday, December 12, 2018 Sheet 24 of 53

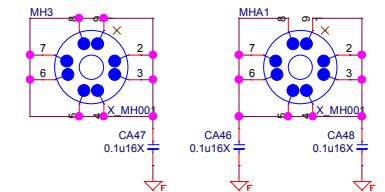
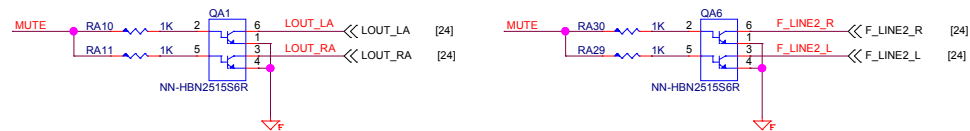
### Rear Line OUT De-POP circuit

De-pop circuit for Rear Line out & Front Headphone out)

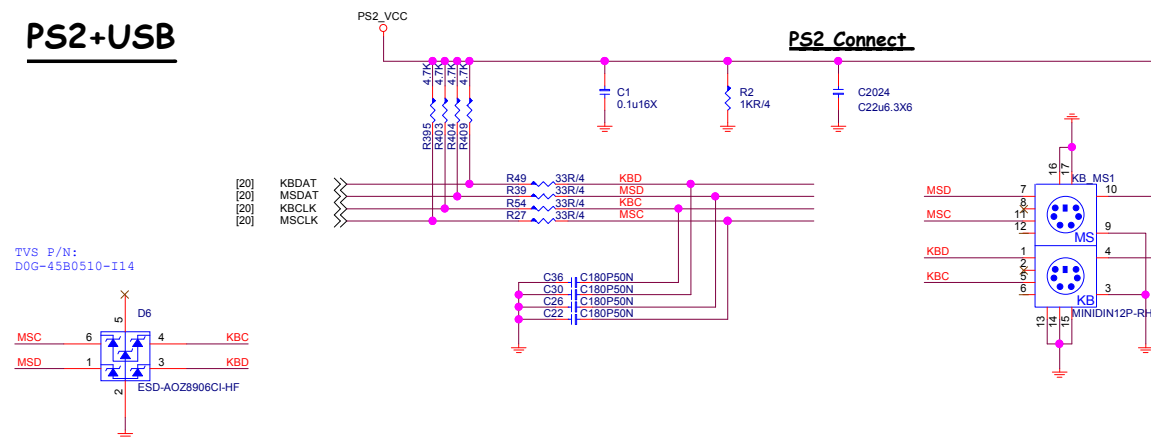


Digital

Analog



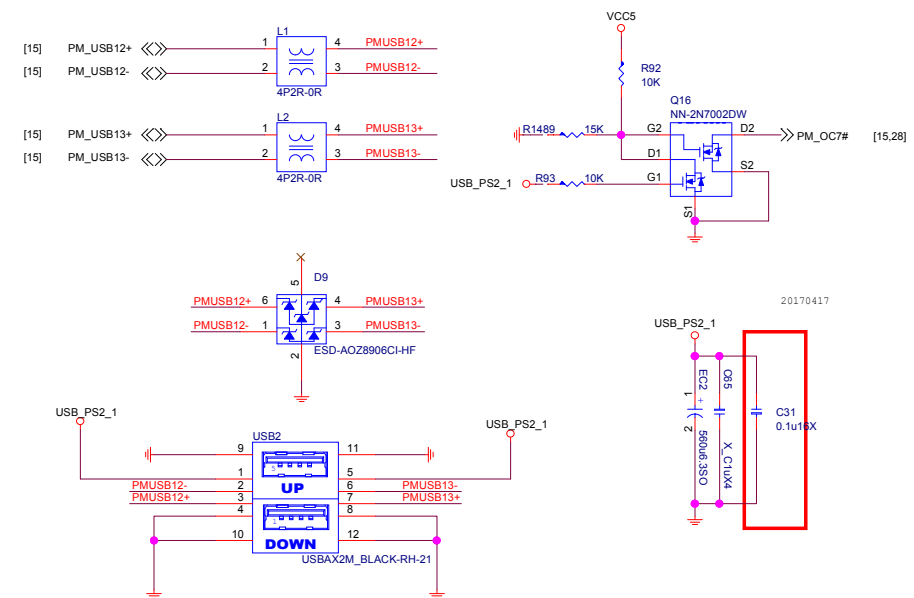
**PS2+USB**



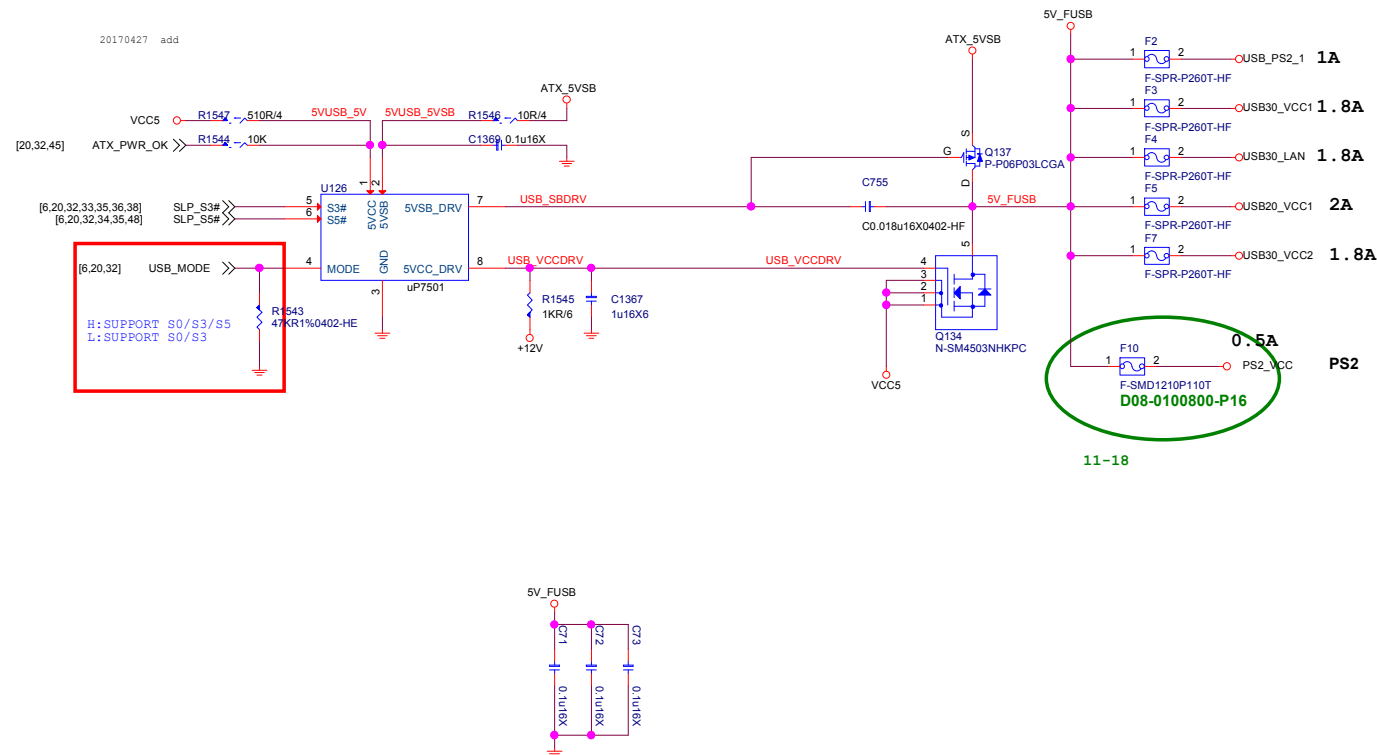
```

layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

```



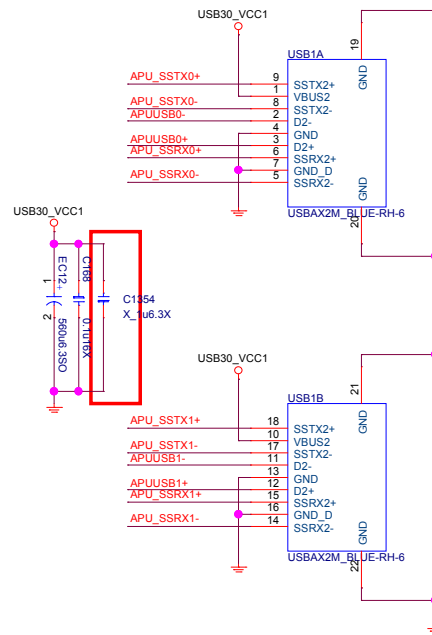
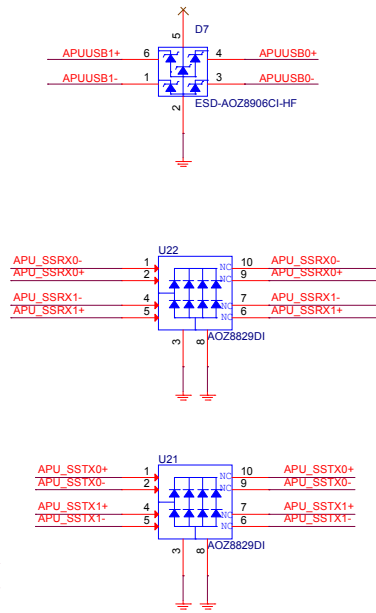
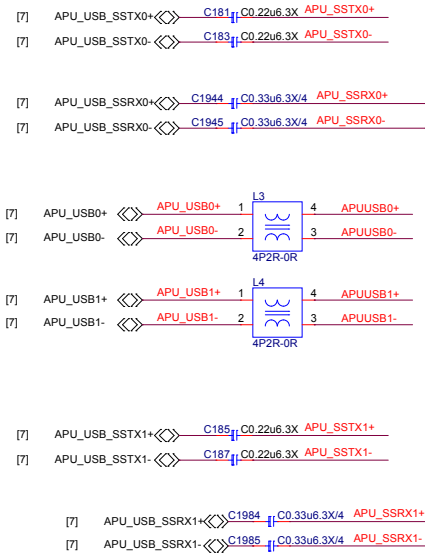
## USB Power



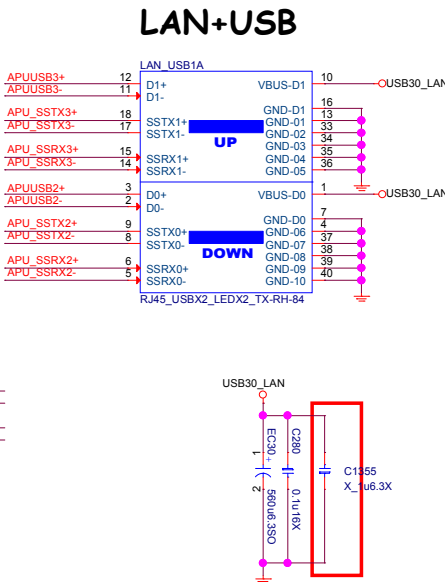
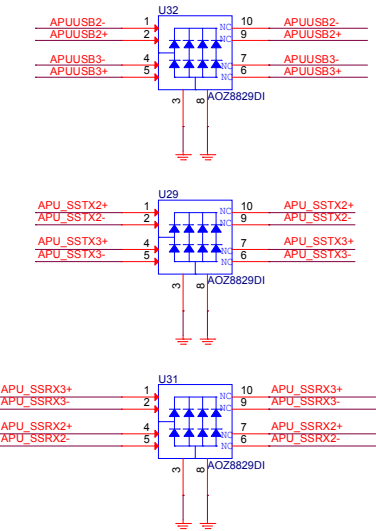
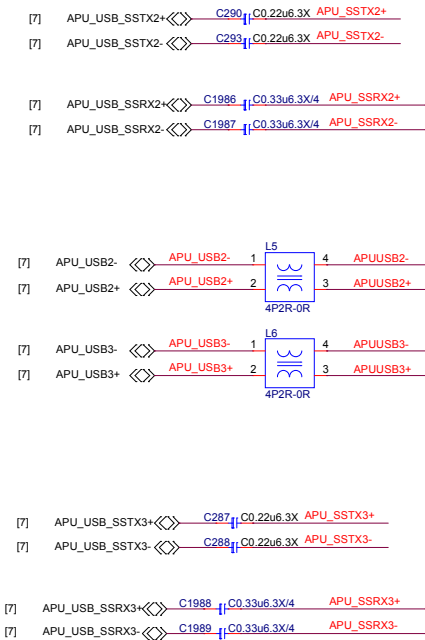
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11-18

## USB 3.0

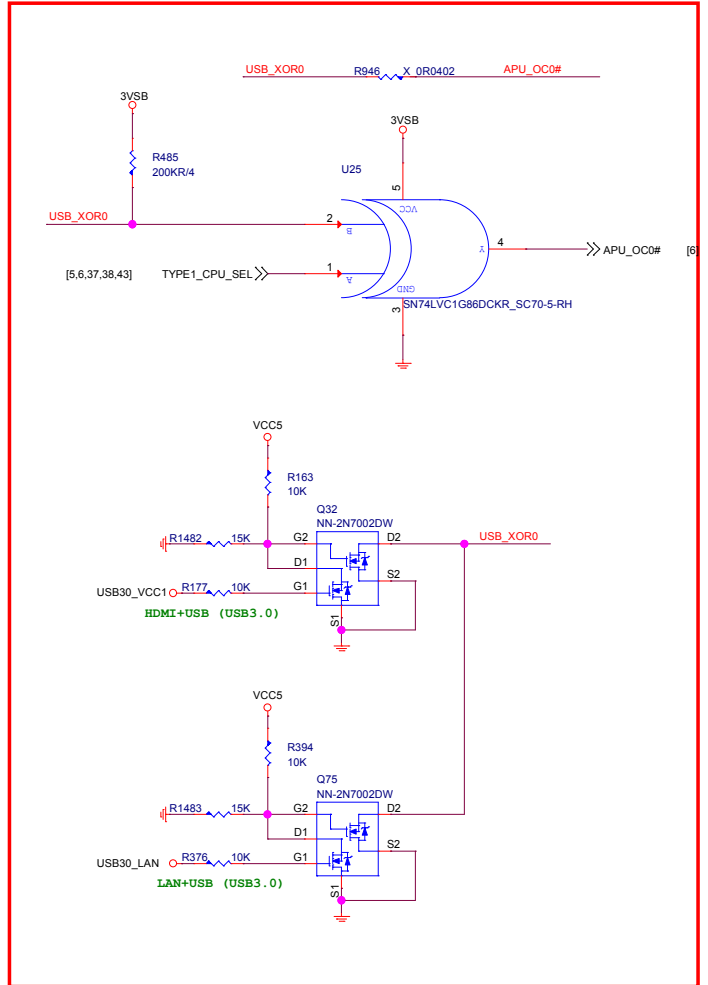


## USB3.1 GEN1



## APU\_USB\_OC

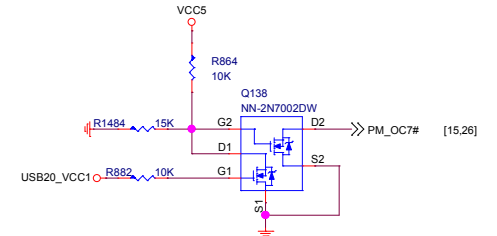
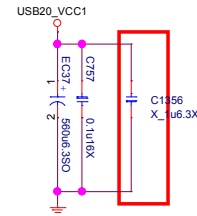
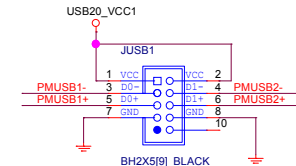
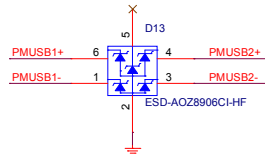
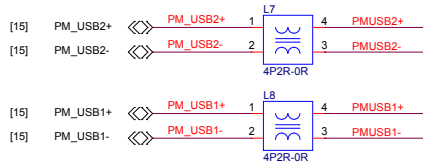
Modify USB\_OC# circuit



	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

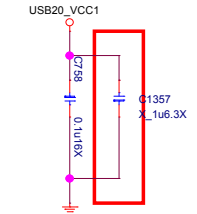
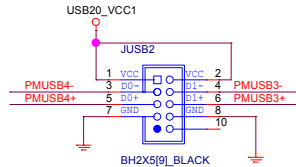
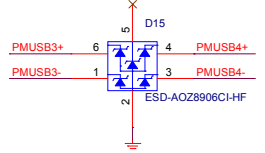
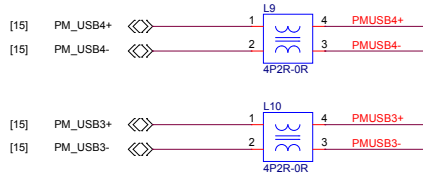
# Front USB2.0 (JUSB1)

5V@1A

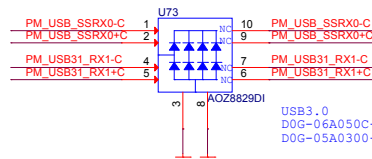
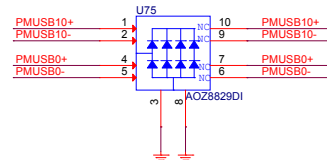
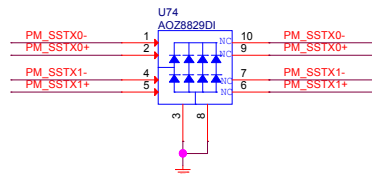
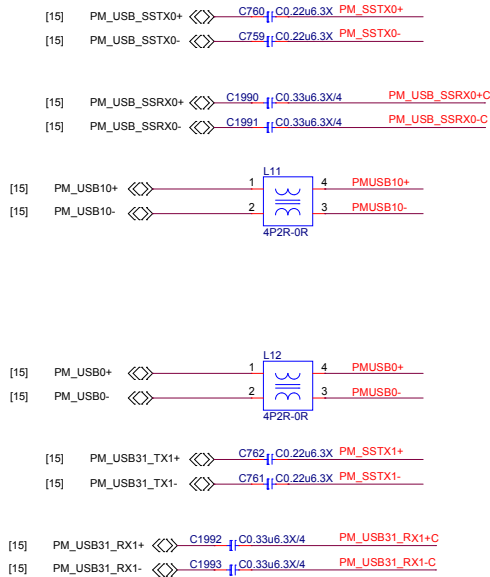


# Front USB2.0 (JUSB2)

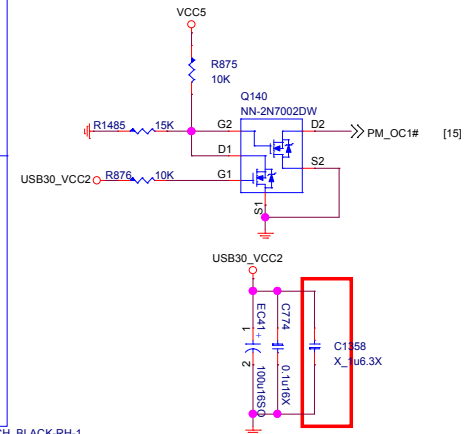
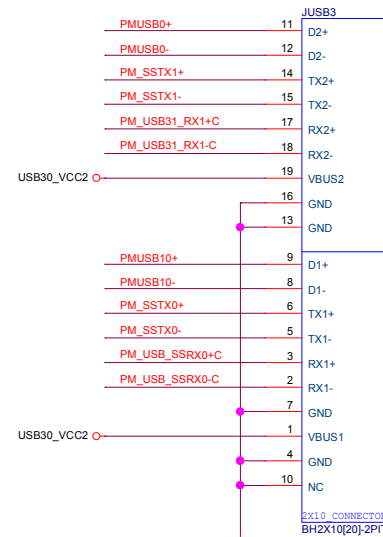
5V@1A



# Front USB3.1 GEN1

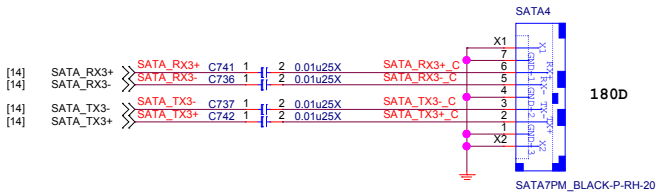
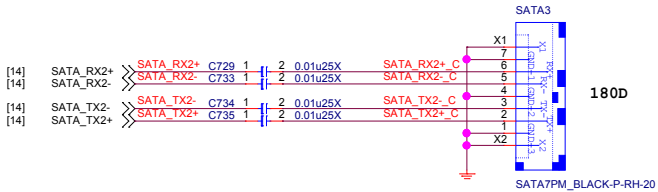
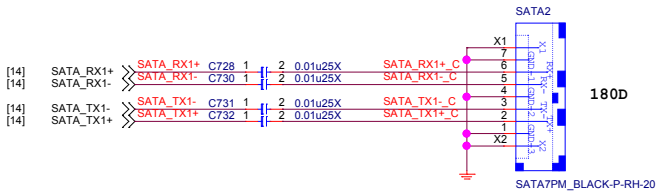
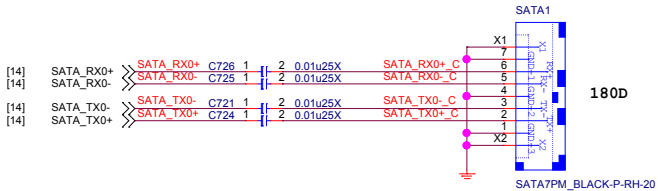


USB3.0  
D0G-06A050C-A68 Main  
D0G-05A0300-I14 AVL  
USB2.0  
D0G-0200529-A68 Main  
D0G-0100619-I05 AVL



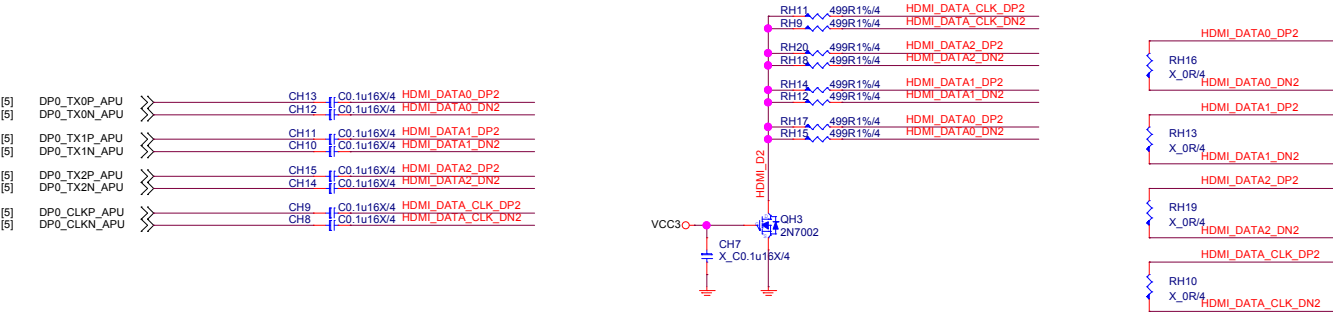


SATA Connector

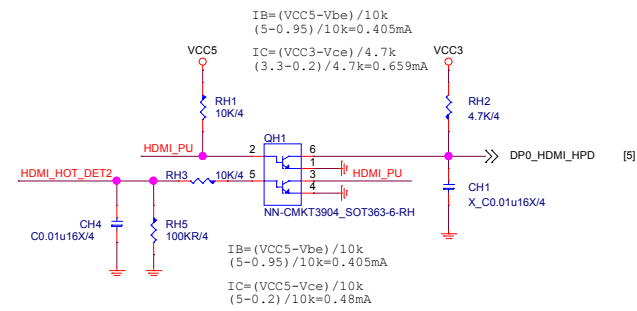


HDMI CONNECTOR

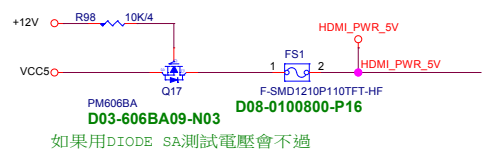
For HDMI 1.4



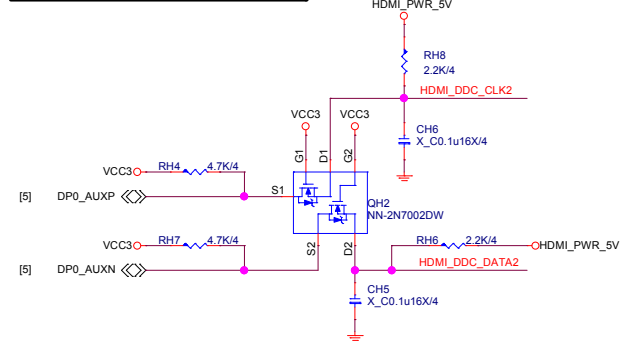
HPD Circuit



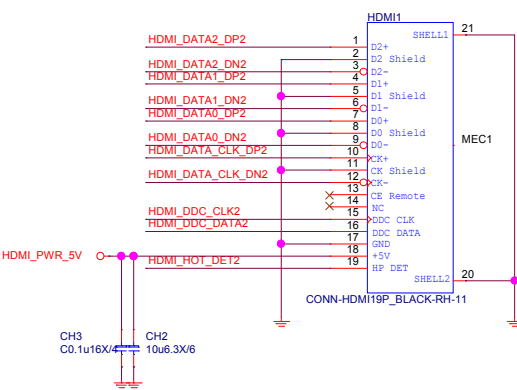
Connector Power



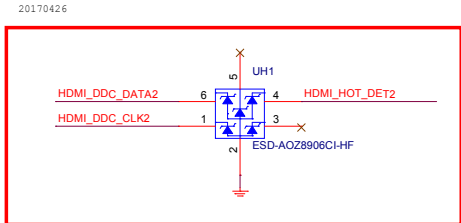
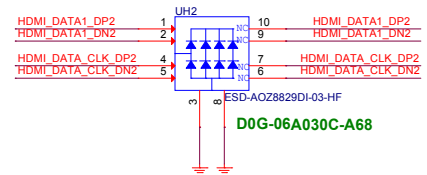
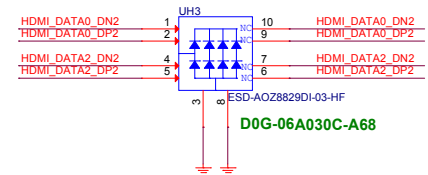
AUX Level Shifter



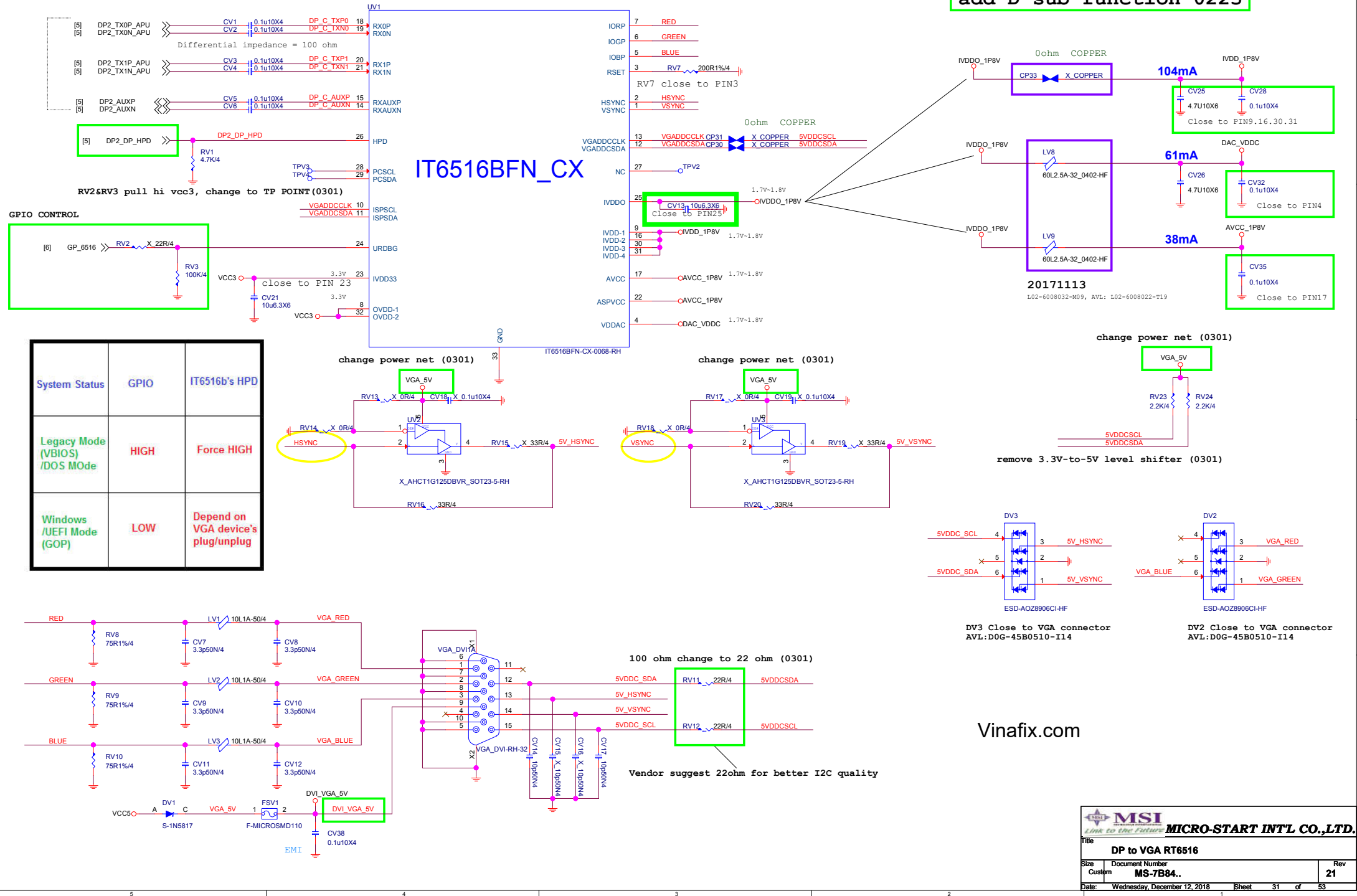
Connector



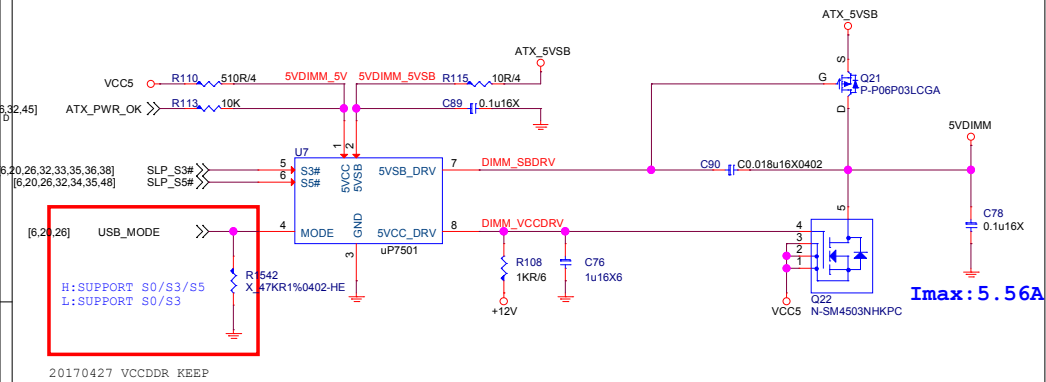
For EMI



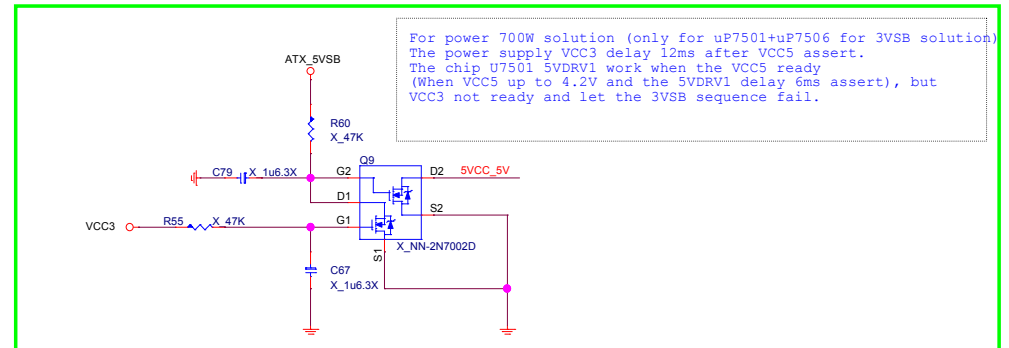
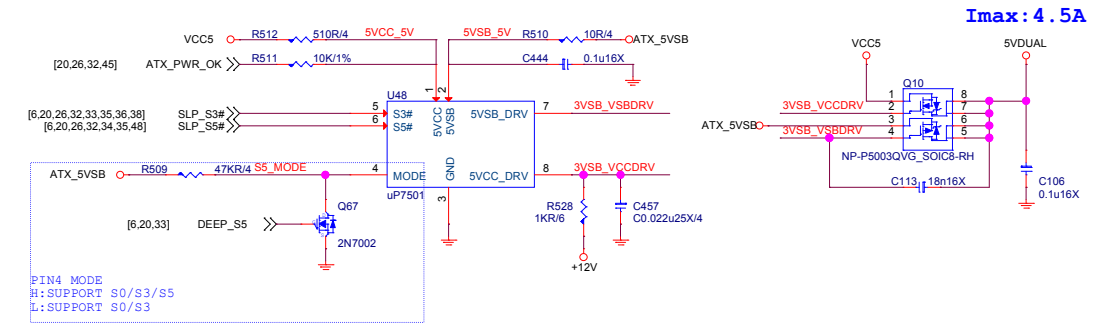
**Note:**  
If connect to eDP port,must confirm whether it support hot plug detection HPD and re-auxtraining



## 5VDIMM FOR DDR

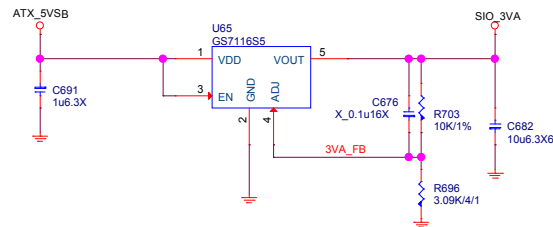


## 5VDUAL For 3VSB、CPU 1.8V、VDDP

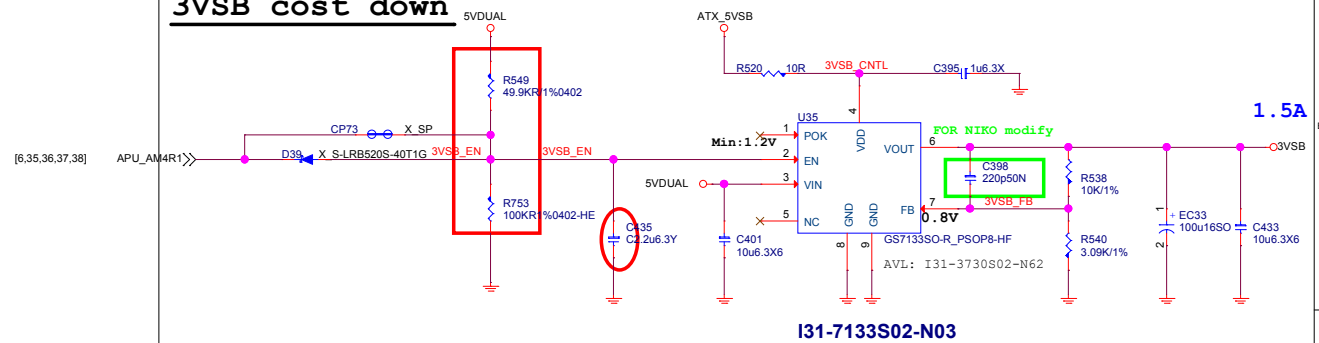


For power 700W solution (only for uP7501+uP7506 for 3VSB solution)  
The power supply VCC3 delay 12ms after VCC5 assert.  
The chip U7501 5VDRV1 work when the VCC5 ready  
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but  
VCC3 not ready and let the 3VSB sequence fail.

## SIO\_3VA



## 3VSB cost down



# FOR Promontory 1.05V\_S0

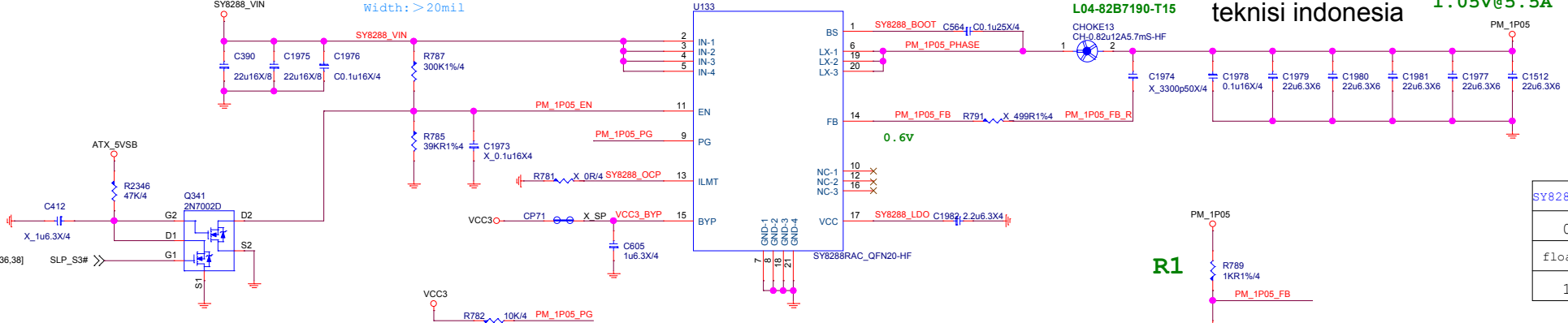
1.05V  
S0:5.5A  
S5:0.05A

Input Current= (5.5A\*1.05V)/12V/0.8=0.6A

OCp=12A

1.05V@5.5A

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R1

R2

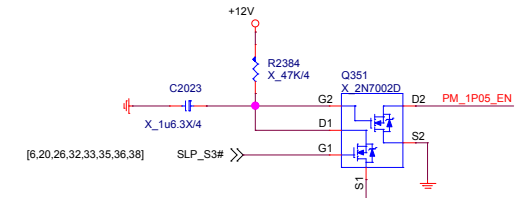
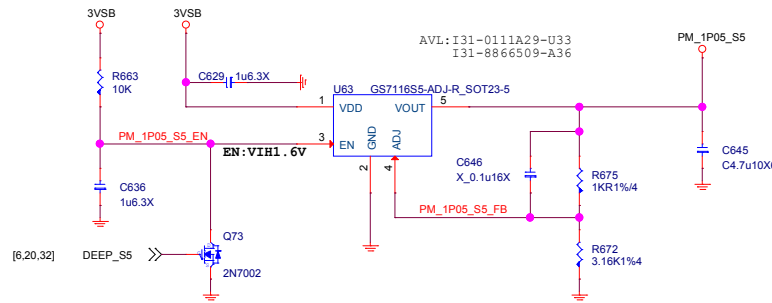
$$V_{out} = V_{ref} * (1 + (R1/R2))$$

$$= 0.6 * (1 + (1K/1.33K))$$

$$= 1.051V$$

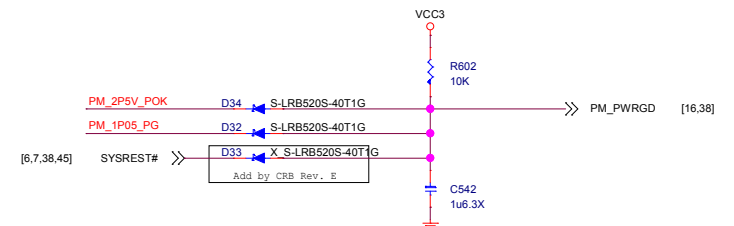
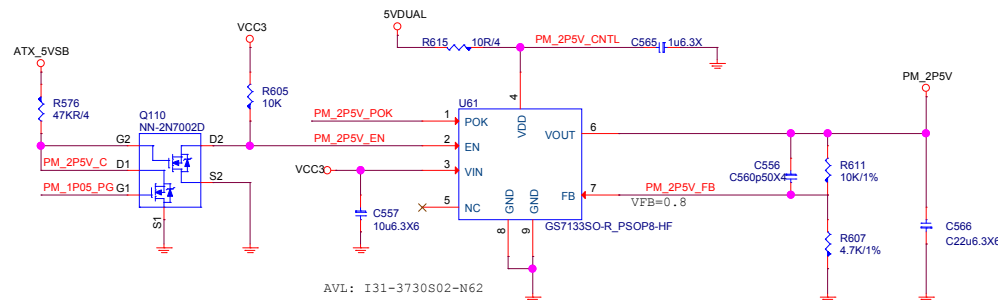
# FOR Promontory 1.05V\_S5

0.05A

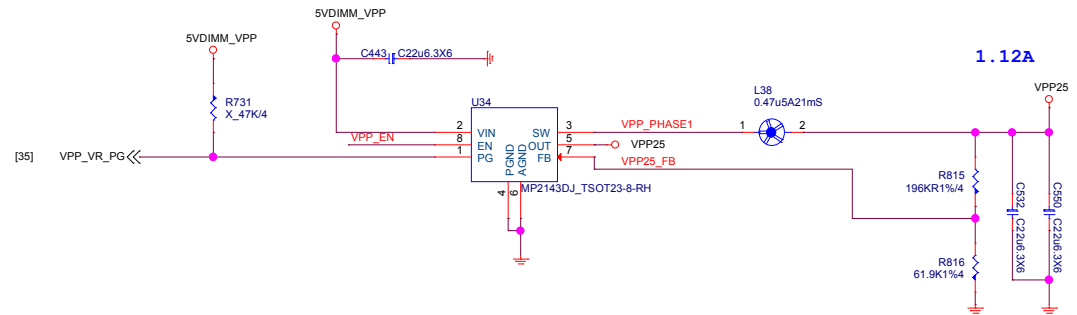
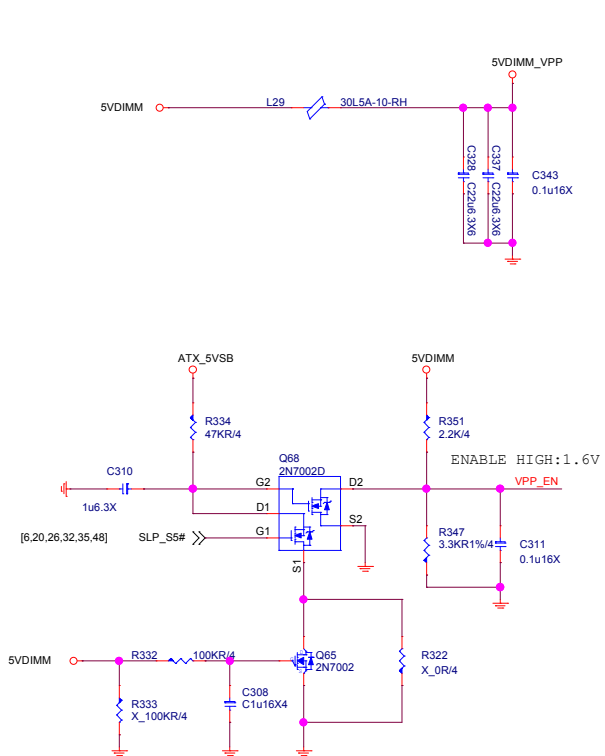


# Promontory-2.5V

2.5V; 900mA

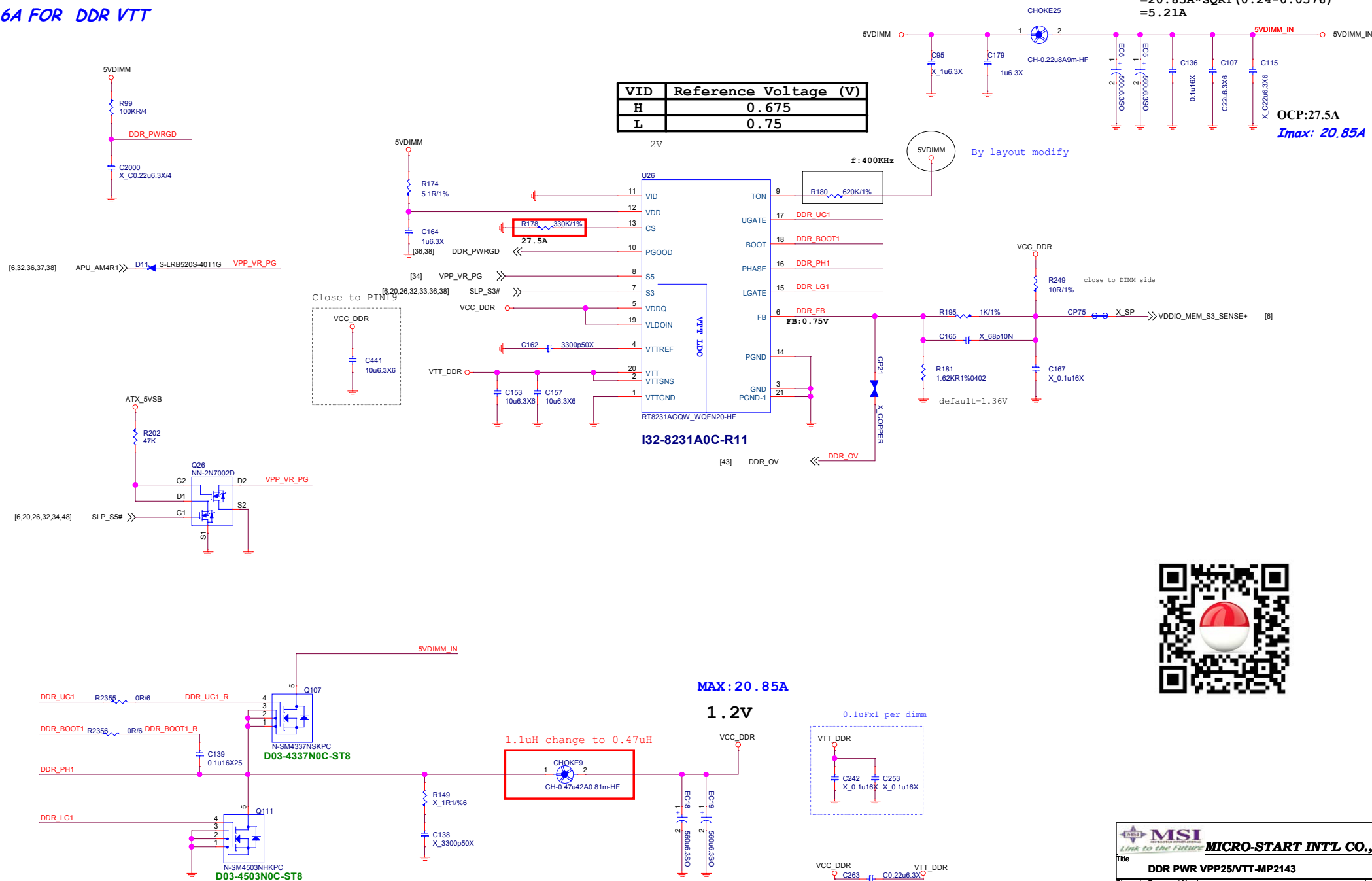


**2DIMM :1.12A FOR DDR VPP2.5V**



15.5A FOR CPU  
4.75A FOR 2DIMM  
0.6A FOR DDR VTT

```
Irms = Iout * SQRT{D/N- (D)^2}
VCCDDR:
D=Vout/Vin=1.2/5=0.24
N=Phase number=1
=20.85A*SQRT(0.24-0.0576)
=5.21A
```





FOR CPU 1.8V S5

0.5A

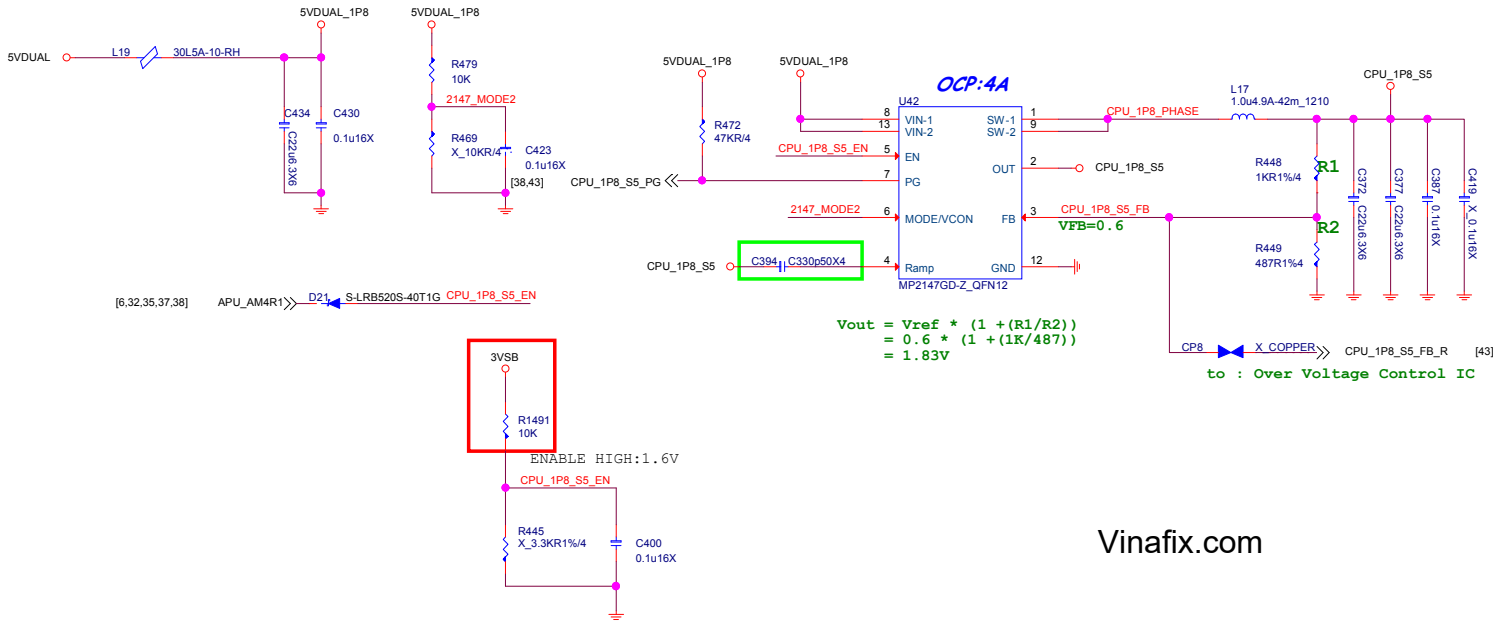
FOR VCCP\_SOC\_S5

0.9A

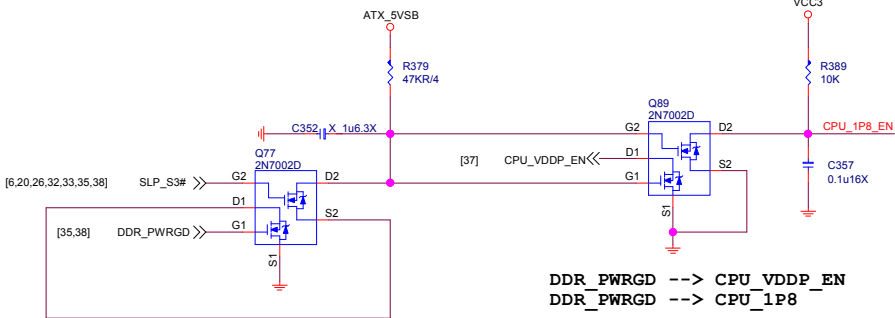
FOR CPU 1.8V S0

2.0A

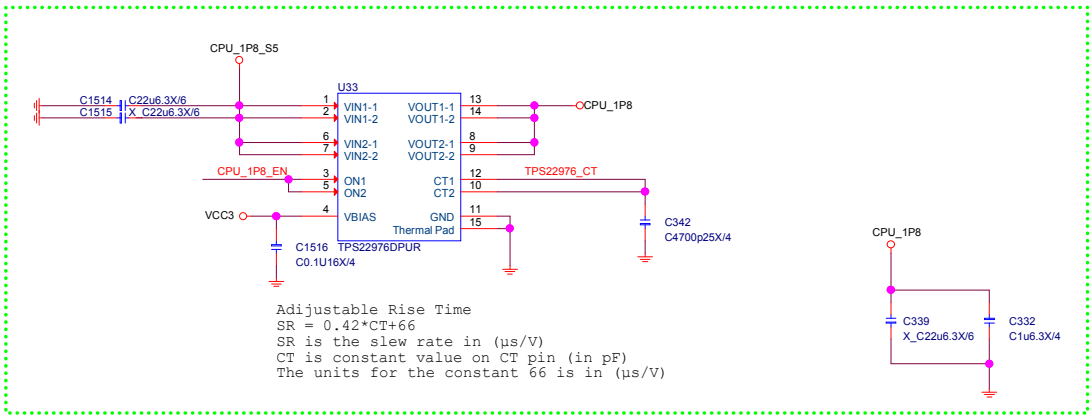
0.5A + 2.0A + 0.9A = 3.4A



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DDR\_PWRGD --> CPU\_VDDP\_EN  
DDR\_PWRGD --> CPU\_1P8\_EN



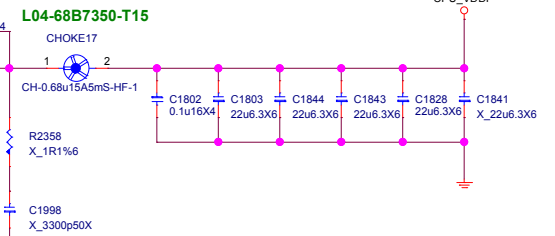
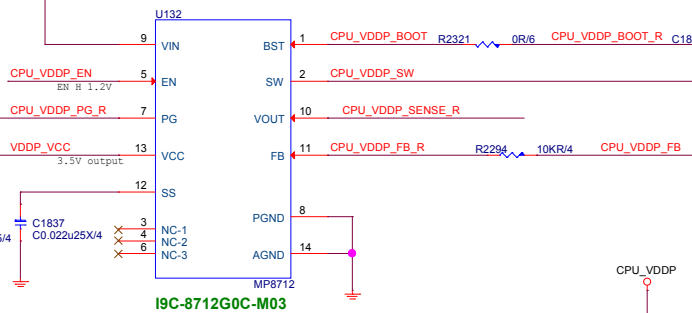
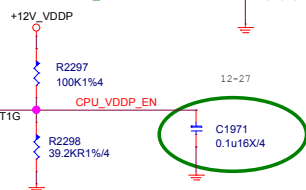
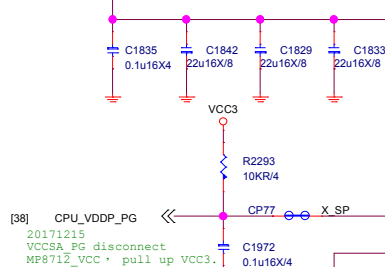
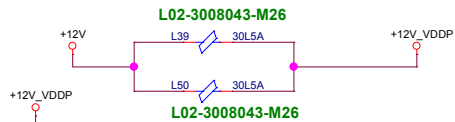
Adjustable Rise Time  
SR = 0.42\*CT+66  
SR is the slew rate in (μs/V)  
CT is constant value on CT pin (in pF)  
The units for the constant 66 is in (μs/V)

## CPU\_VDDP\_S0

1.05V/0.9V@S0:8.5A

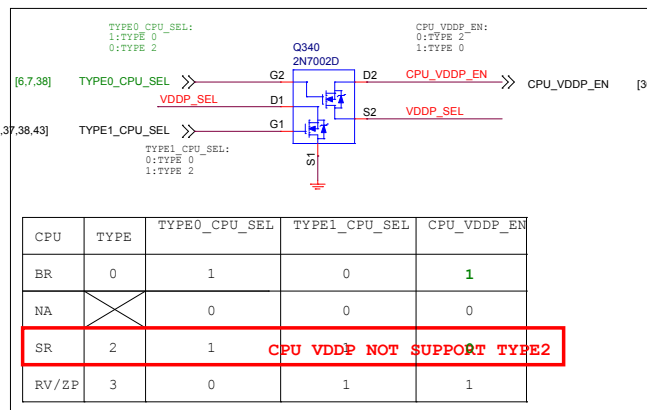
S0:8.5A  
S5:1A  
OCP=14A

Input Current= (8.5A\*1.05V)/12V/0.8=0.93A



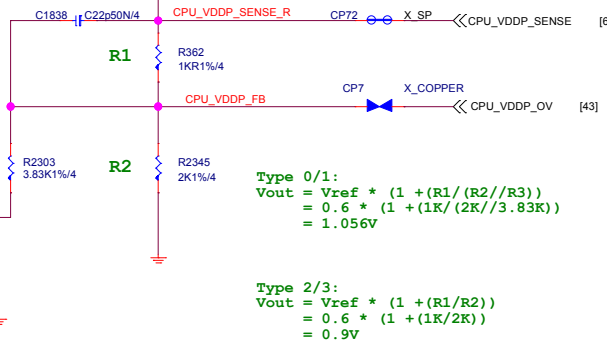
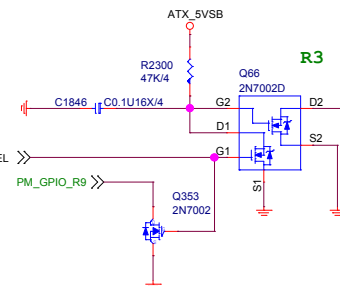
OCP=14A

1.05V, 8.5A



AM4\_CPU\_SEL  
0:Type 0/1 =>1.053V  
1:Type 2/3 =>0.9V

PM\_GPIO\_R9  
Page 17 pull high  
1:Type 0/1 1.05V  
0:Type 2/3 0.9V

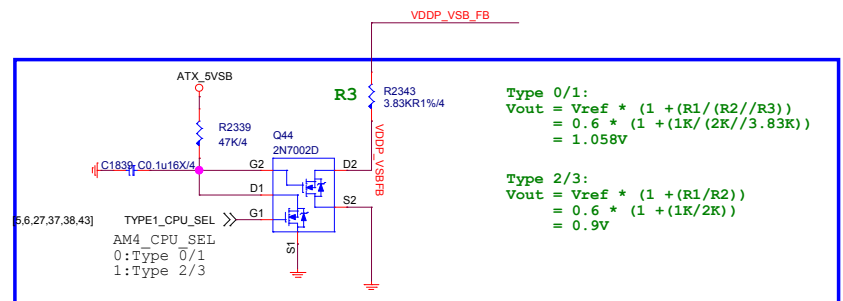
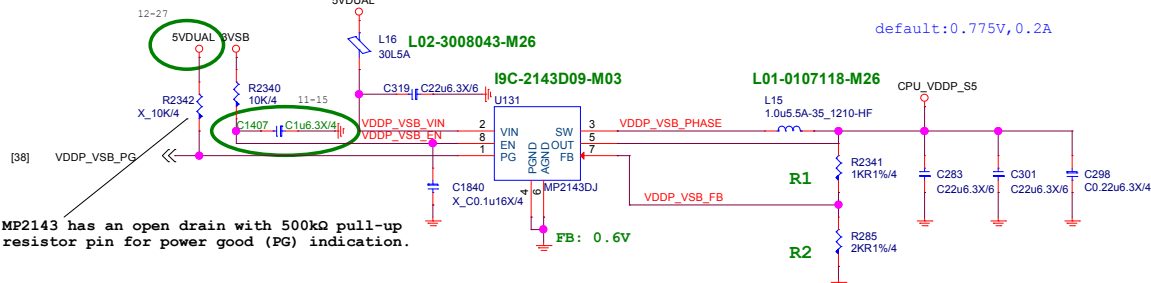


## CPU\_VDDP\_S5

1.05V/0.9V  
S5:1A

Input Current=0.04A

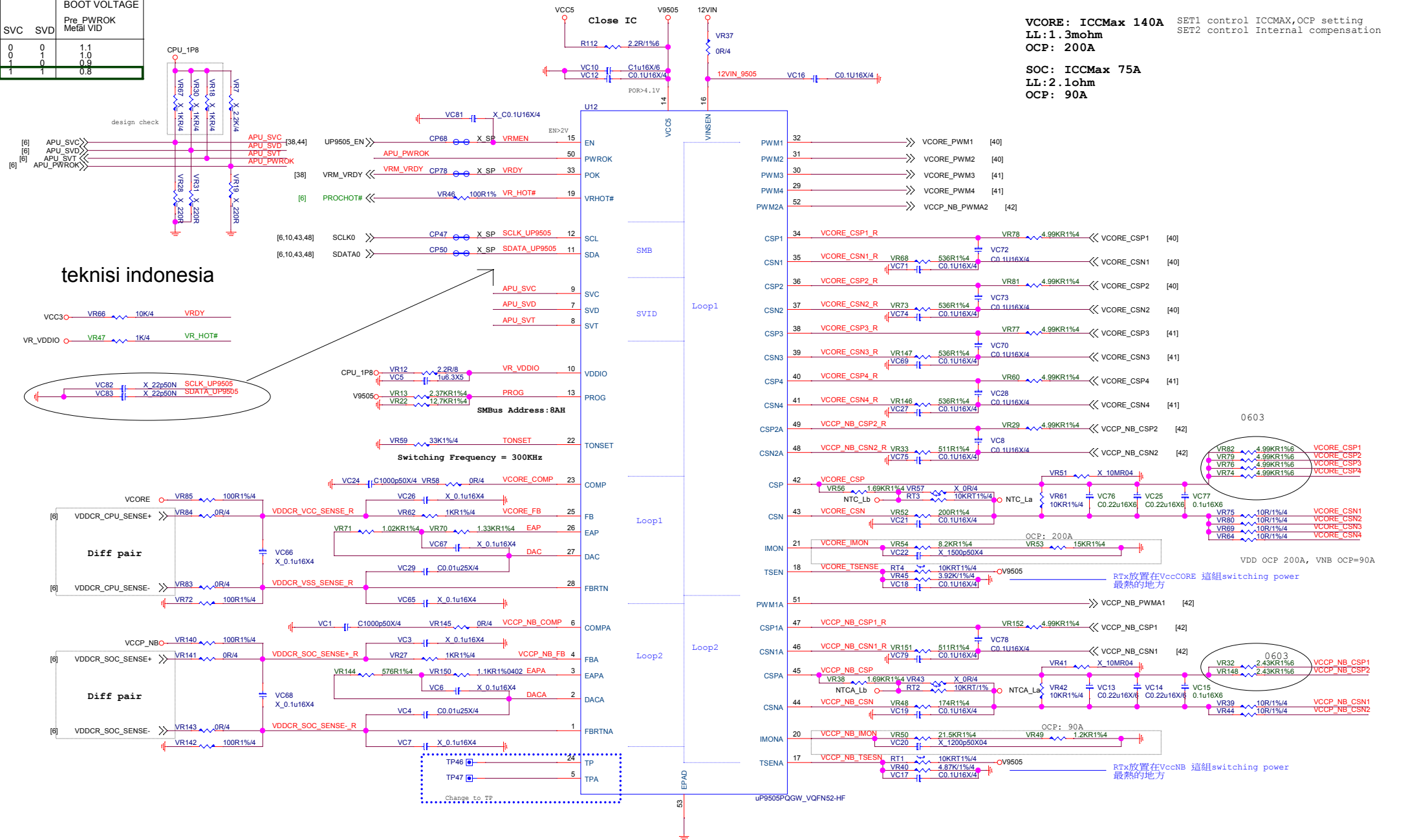
default:0.775V, 0.2A

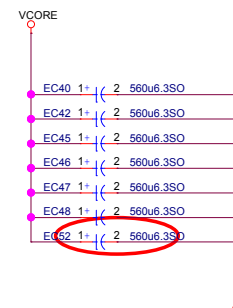
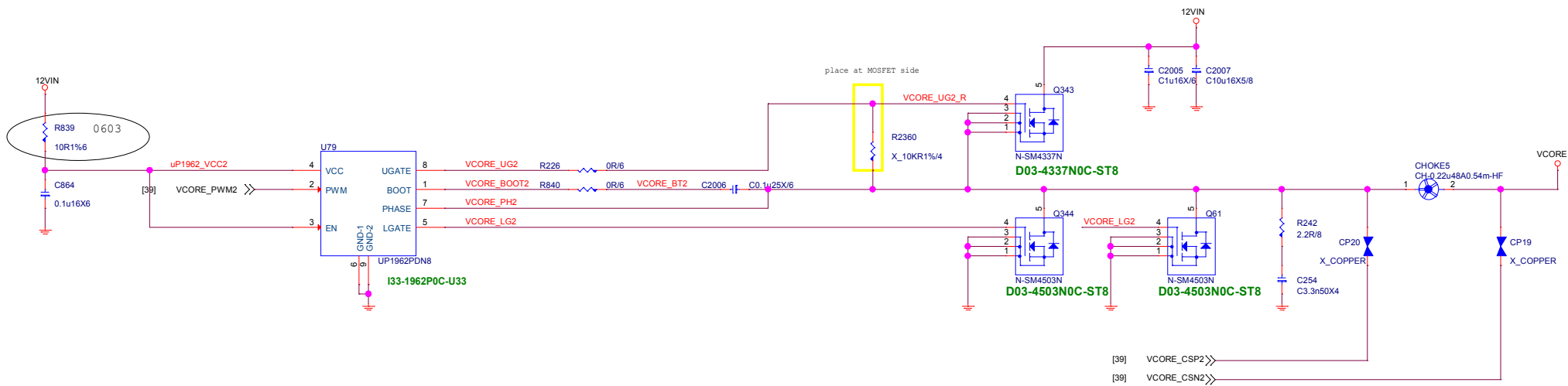
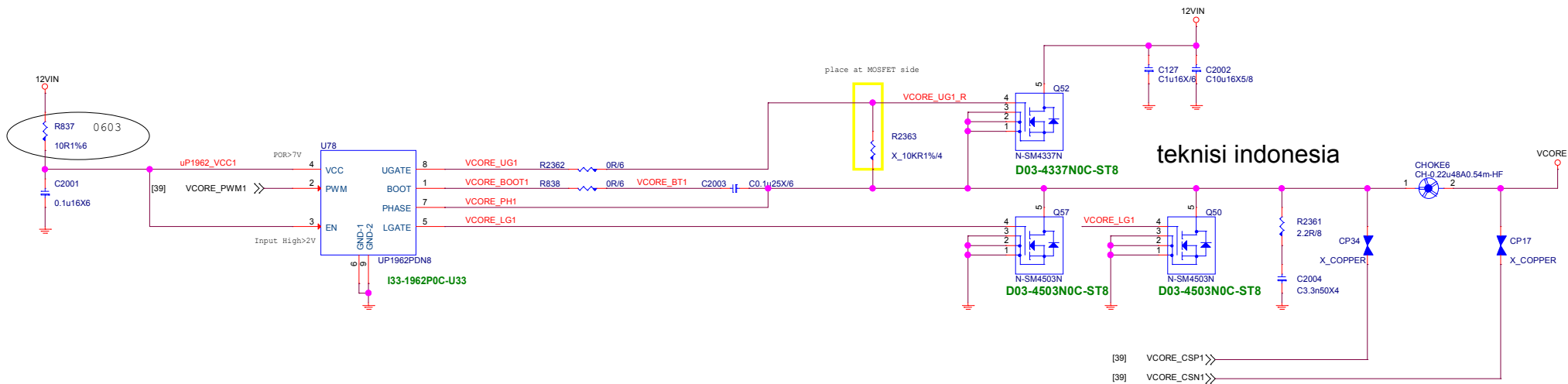


MP2143 has an open drain with 500kΩ pull-up resistor pin for power good (PG) indication.

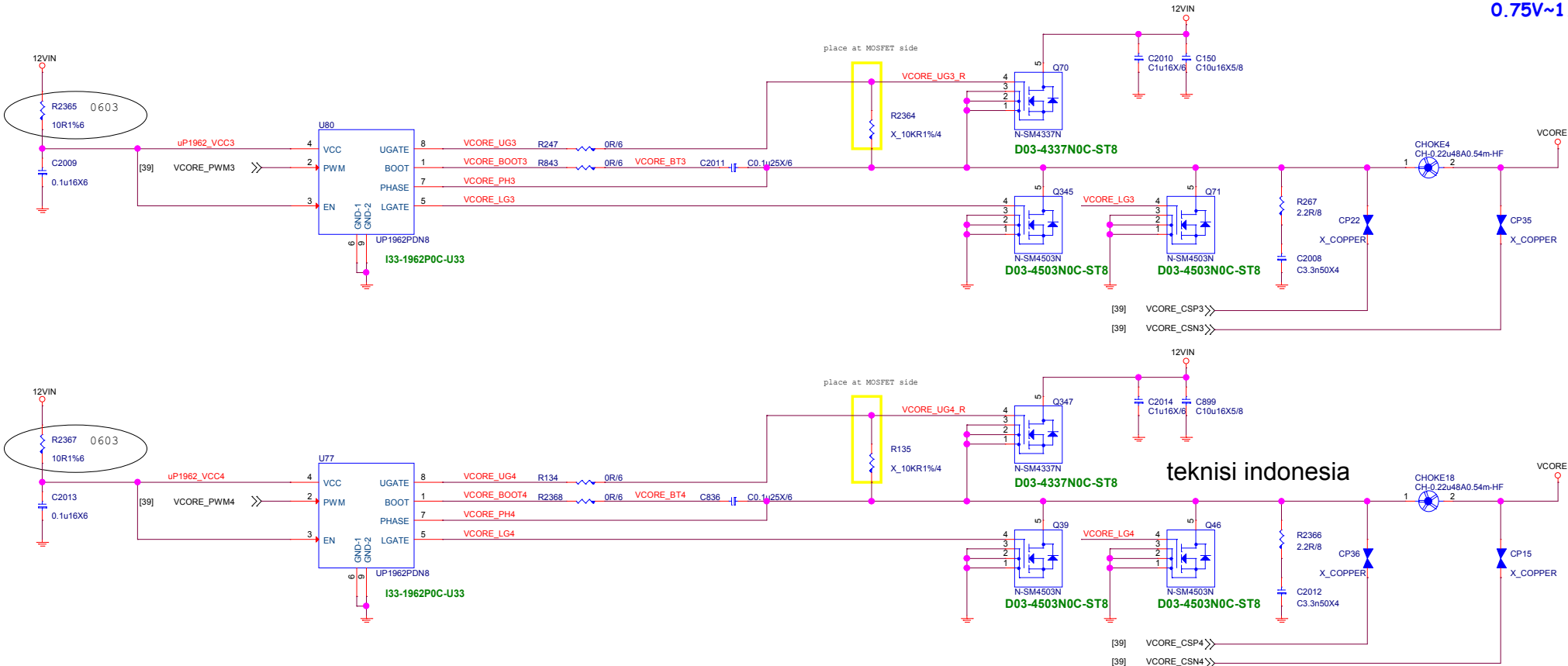


		BOOT VOLTAGE
SVC	SVD	Pre PWROK Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



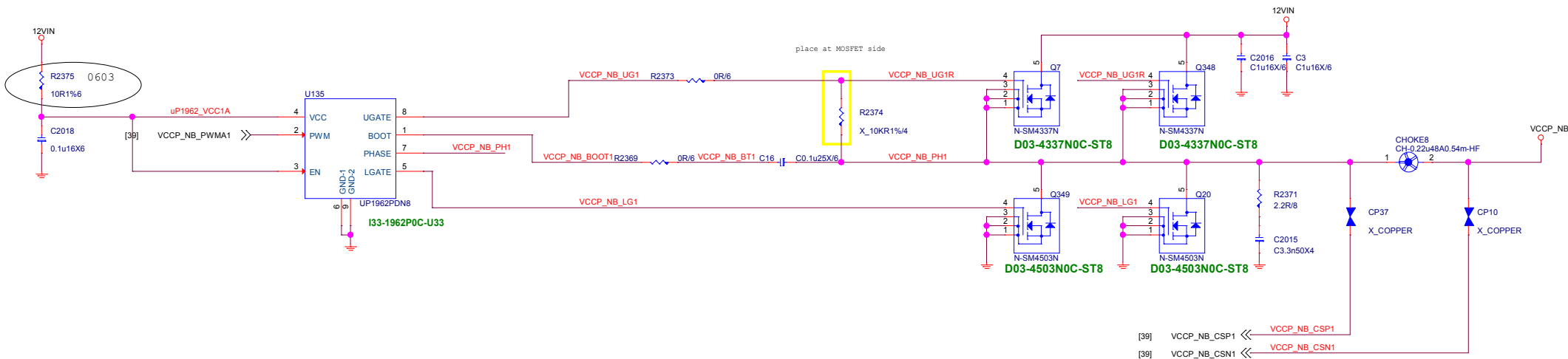


0.75V~1.2V

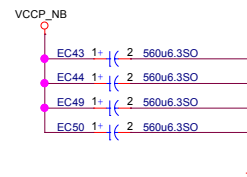


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0.00625V~1.55V



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FOR  
VCCP\_SOC\_S5  
0.9A

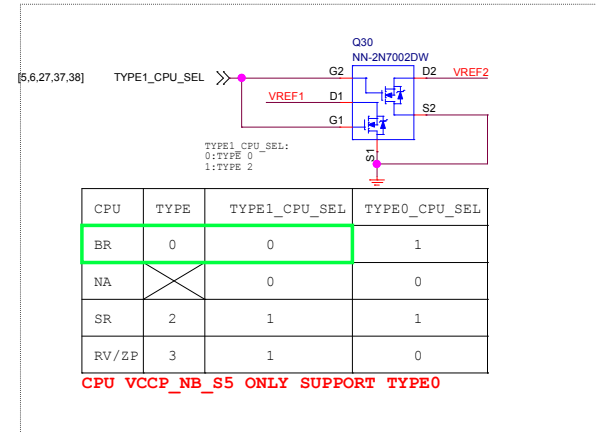
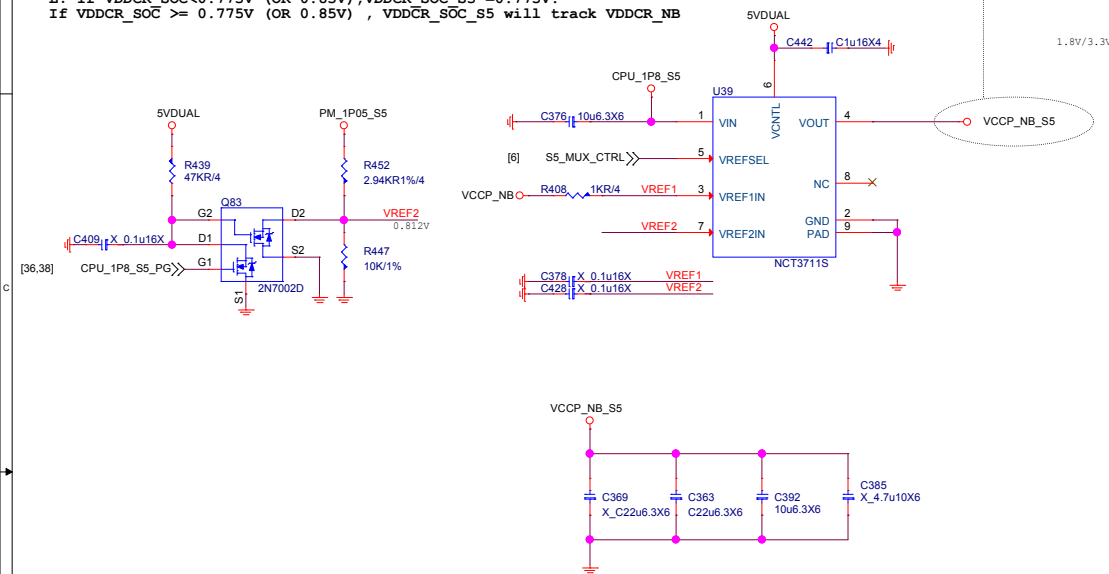
(VDDCR\_SOC\_S5 is only used for AMD TYPE0)

TYPE0 Only

S5\_MUX\_CTRL  
HIGH:S0  
LOW: S3/S5

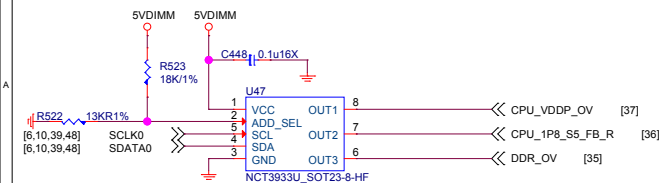
H: +VDDCR\_FCH ALW will track VDDNB  
L: If VDDCR\_SOC<0.775V (OR 0.85V), VDDCR SOC S5 =0.775V.  
If VDDCR\_SOC >= 0.775V (OR 0.85V) , VDDCR\_SOC\_S5 will track VDDCR\_NB

(VDDCR\_SOC\_S5 is only used for AMD Family 15h Models 60h-6Fh processors) Bristol Ridge TYPE0

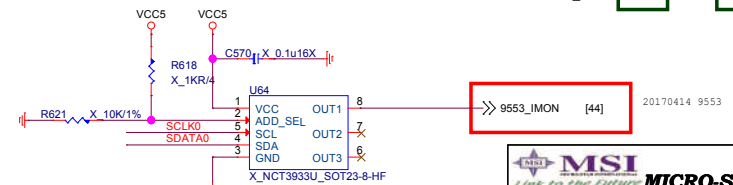


## Over Voltage Control IC

0x26: RH=18K, RL=13K



0x2A: RH=OPEN, RL=10K



## UPI VOLTAGE CONSOLE

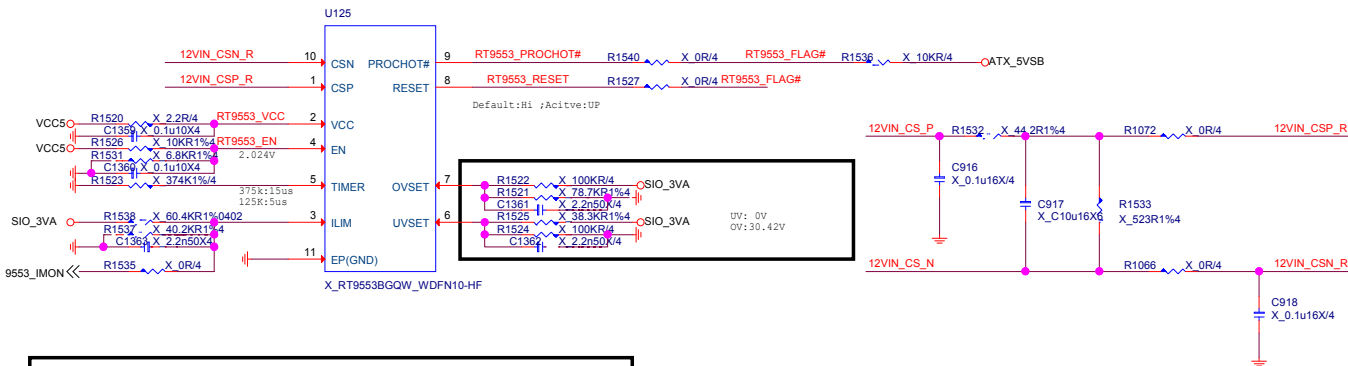
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

MSI Link to the Future		MICRO-START INT'L CO.,LTD.	
Title CPU Power NB Switch / NCT3933 OV			
Size Custom	Document Number MS-7B84..		Rev 21
Date Wednesday, December 12, 2018	Sheet 43	of 53	

# RT9553 CURRENT SENSE

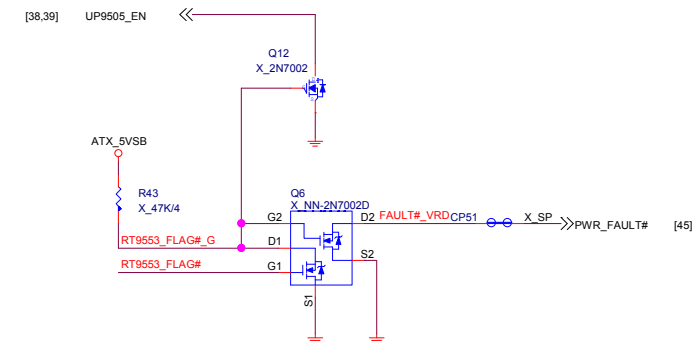
VCORE EDC MAC 125A

NB EDC MAX75A

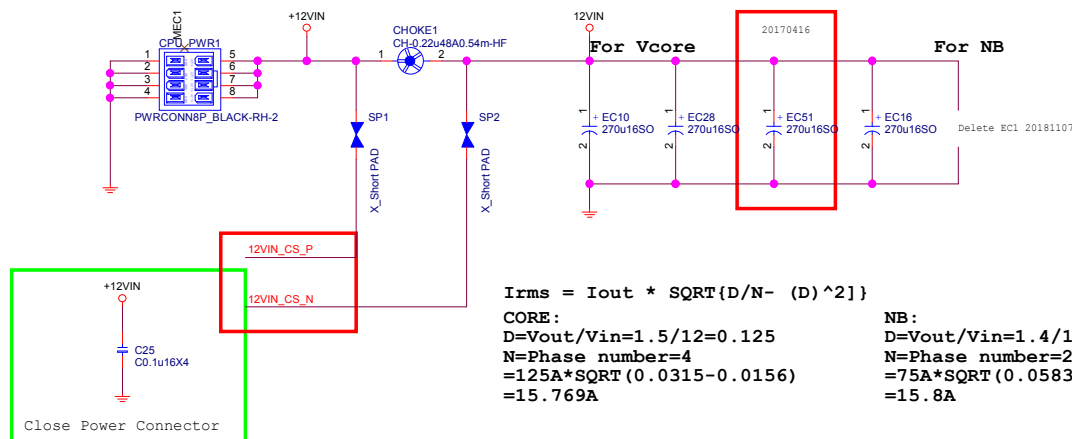


OCP:30A  
Real OCP:30.05A  
R17+R18>100k V<sub>sio\_3va</sub>= 3.38V Rdcr= 0.5 mohm

$I_{3933\_imon} * [R17 * R18 / (R17 + R18)] = I_{step} * Rdcr * 100$   
I3933\_imon= 10uA/step  
Istep=4.785A



## CPU POWER CONNECTOR

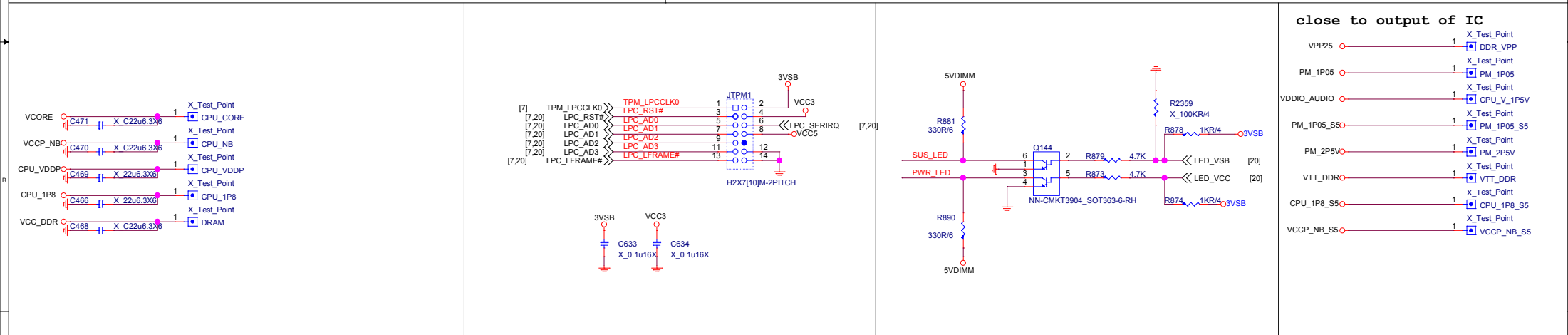
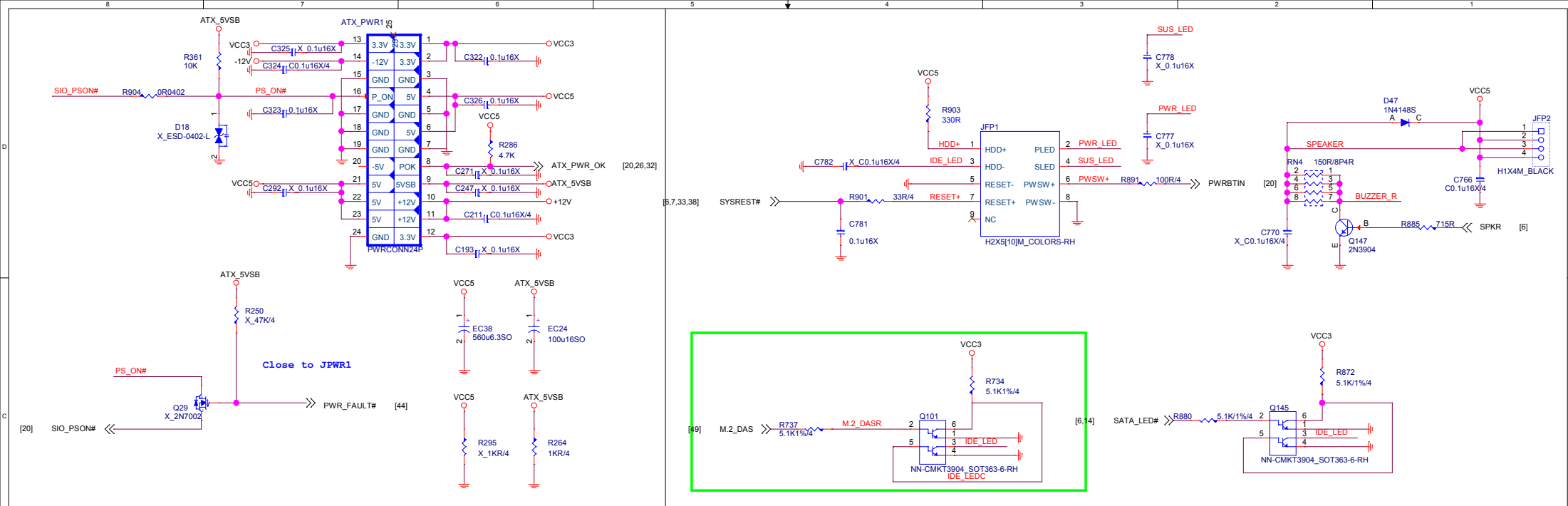


$$I_{rms} = I_{out} * \sqrt{D/N - (D)^2}$$

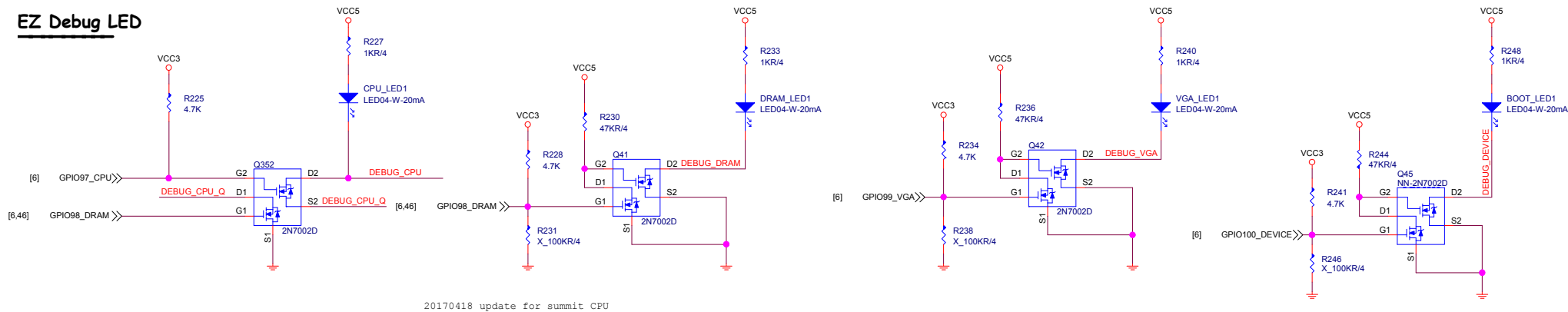
CORE:  
D=V<sub>out</sub>/V<sub>in</sub>=1.5/12=0.125  
N=Phase number=4  
=125A\*SQRT(0.0315-0.0156)  
=15.769A

NB:  
D=V<sub>out</sub>/V<sub>in</sub>=1.4/12=0.1166  
N=Phase number=2  
=75A\*SQRT(0.0583-0.0136)  
=15.8A

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## EZ Debug LED

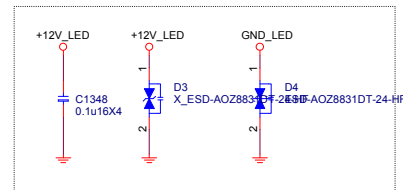
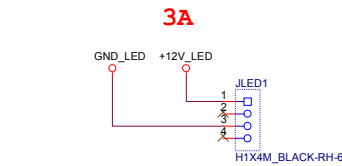
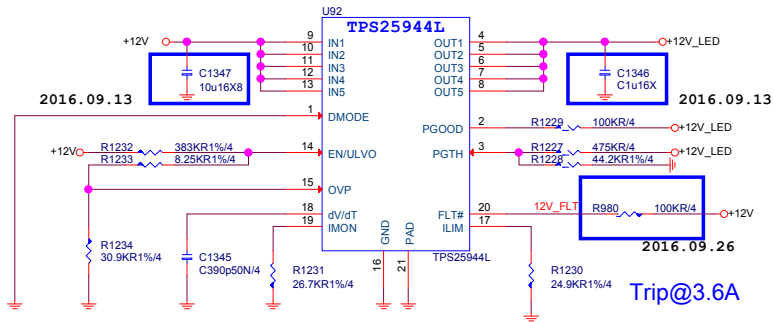


## LED Control by SIO

### JLED

2016.07.06 Use TPS25944L

LED_GPIO	GPIO97	GPIO98	GPIO99	GPIO100
	GPI FULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

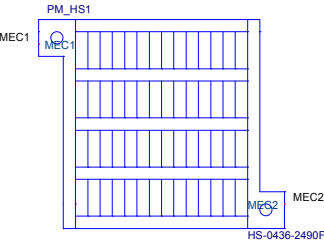


close to JLED1

## AM4 APU Detect LED Circuit

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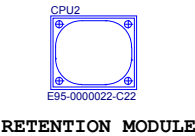
HEAT SINK



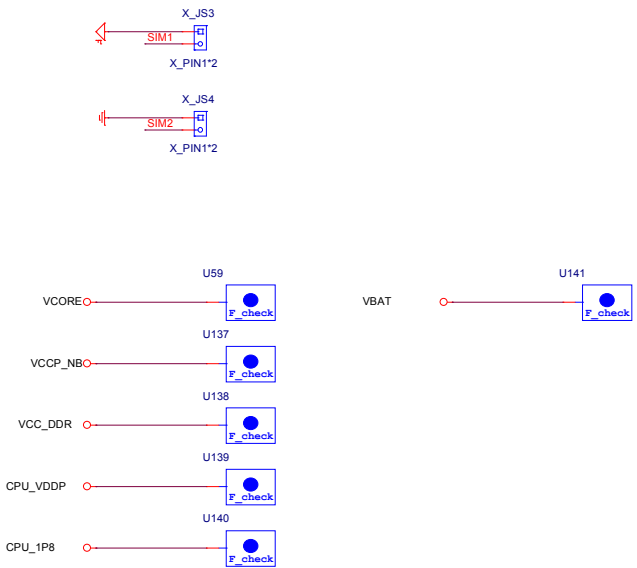
5010 Level



CPU Socket

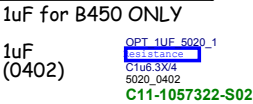


Simulation



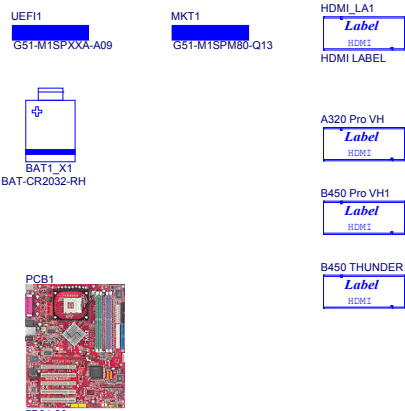
60 Level

5020 Level



CAP USE N07 for A320/B450 SKU

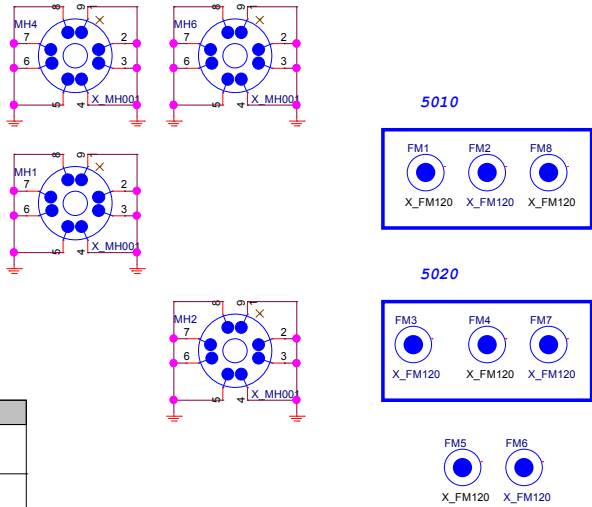
MANUAL PART



PK0-07B8420-G37,精成-深圳,22,寶安恩斯邁廠 (MSIS)

PK0-07B8420-E48,競華,23,寶安恩斯邁廠 (MSIS)

Optics Orientation Holes



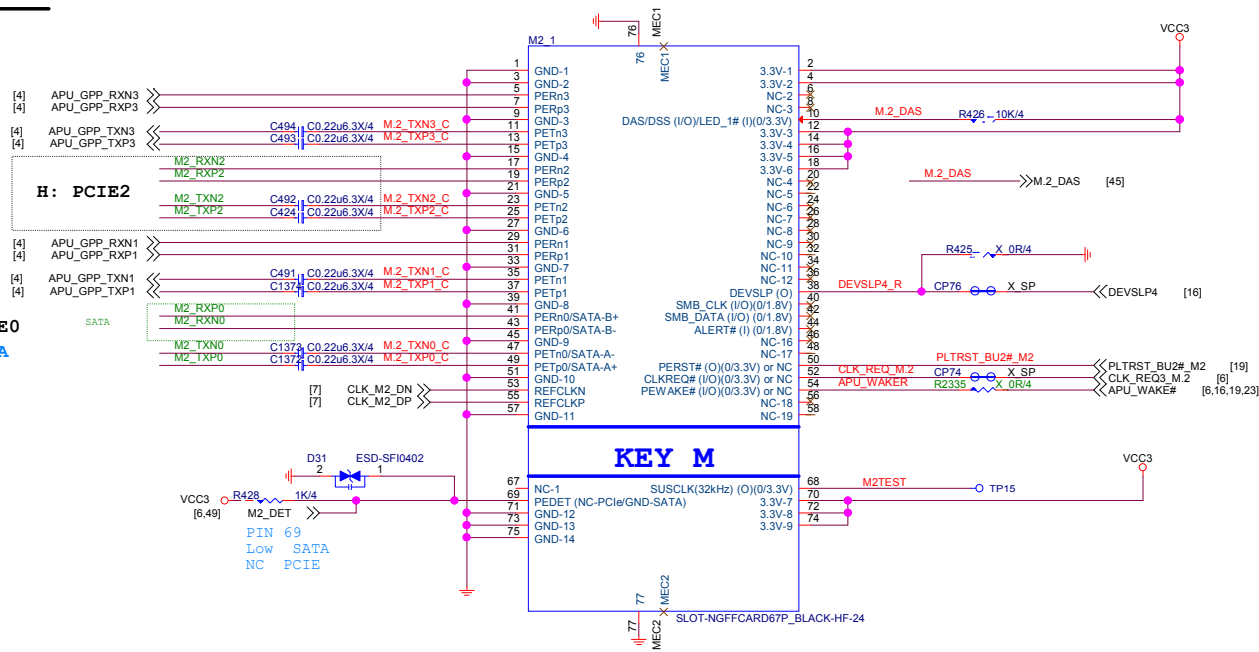
OPT	Configure	BOM	Function
		601-7B84-A01	XXXX



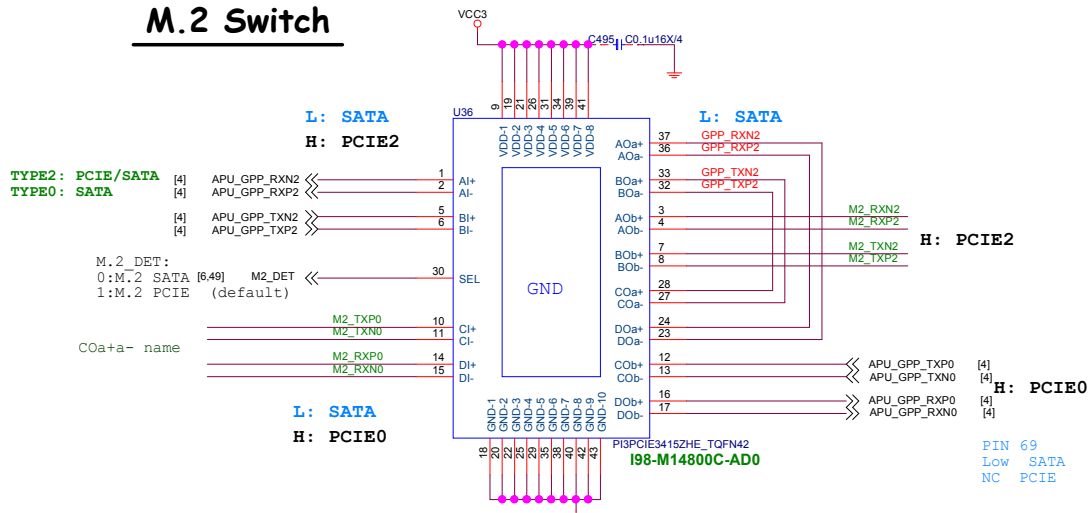
# M.2 Connector

3.3V@2.5A

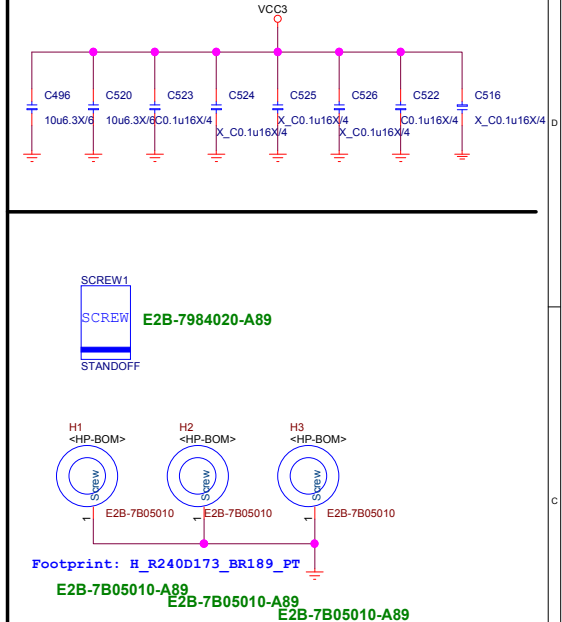
H: PCIE0  
L: SATA



## M.2 Switch



3.3V@2.5A



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